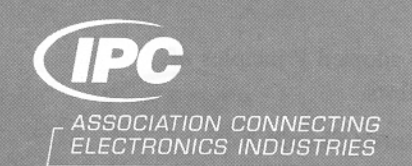


IPC-2141

Controlled Impedance Circuit Boards and High Speed Logic Design

IPC-2141

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A standard developed by IPC

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Developed by the Controlled Impedance Task Group (D-21c) of the High Speed/High Frequency Subcommittee (D-21) of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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Controlled Impedance Circuit Boards and High Speed Logic Design

1.0 Scope

This guide is intended to be used by circuit designers, packaging engineers, printed board fabricators, and procurement personnel so that all may have a common understanding of each area.

The goal in packaging is to transfer a signal from one device to one or more other devices, through a conductor. High-speed designs are defined as designs in which the interconnecting properties affect circuit performance and require unique consideration.

2.0 References

The following standards contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

IPC T-50 Terms and Definitions for Printed Circuits

IPC-L-108 Specification for Thin Laminates, Metal Clad Primarily for High Temperature Multilayer Printed Boards

IPC-L-109 Specification for Glass Cloth, Resin Preimpregnated (B-Stage) for High Temperature Multilayer Printed Boards

IPC-L-115 Specification for Plastic Sheet, Laminated Metal Clad for High Temperature Performance Printed Boards

IPC-TM-650 Test Methods Manual
T.M. 2.5.5.7 Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR[1]

IPC-D-317 Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

IPC-2220 Design of Organic Printed Boards and Printed Board Assemblies

The references presented in the bibliography may provide more comprehensive treatment of the subject.

3.0 Engineering Design Overview

Packaging of electronic equipment has traditionally been an area for mechanical considerations. Packaging design is becoming more complex as today's electronics technologies are available in greater switching speed and higher density per chip. Individual chips have greater numbers of connections in smaller chip package sizes. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. Controlled impedance circuit boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily have been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor with interconnections specified in to/from wire listing or net lists. Electrical conductor signals were routed with only a few concerns, that continuity was maintained between points, conductors had sufficient copper for the current and clearance was maintained to prevent voltage breakdown. Aside from providing a good electrical path, the electrical performance of the signal was not a major concern.

Advances in digital integrated circuits have introduced new devices with extremely fast rise times which are housed in high density microelectronic packages. In order to optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance.

With recent advances in semiconductor processing technology, CMOS outputs have output impedance approaching the ECL (5-6 ohms) and can switch 50 ohm lines in as little as 1 nonosecond from one logic level to the other, a swing of 5 volts. These fast edges demand all of the concern normally given the GaAs and ECL logic families.

3.1 Device Selection

Device technology options include TTL, Schottky TTL, CMOS, ECL and GaAs, each with its own set of power requirements, operating temperature range, density of chip, input impedance, output impedance, signal threshold levels, noise sensitivity, response time and output pulse rise/fall time. Many designs will have mixed technology where SMT and through-hole packaging is intermixed with TTL, CMOS and ECL logic that may require multiple line widths (impedance values) on the same circuit layer or may compromise on a single conductor width that can provide enough margin for the different logic families.

1. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

Chips can be individually mounted on a large board or assembled into small boards or multichip modules mounted onto large boards. Large systems may require several large board assemblies with another level of interconnect. Noise, timing, and signal degradation will accompany transitions from one packaging level to the next.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated-through holes in the board, as in dual in-line packages, to a series of lands for surface mount devices. Requirements for component packaging are dependent on many factors including space, economics, electrical performance and reliability, as well as the predominant packaging style of the assembly. The components must be provided in a style that is compatible with the assembly processes used to manufacture the printed board assembly.

The component package must be considered when designing for high speed. In passive components the predominant factor will be the lead length as leads provide additional inductance and capacitance that will affect propagation speed and switching transients. To minimize these effects the leads may be as short as possible . Surface mount devices can provide leadless packages which can be directly mounted to the interconnecting substrate.

Note: Component data sheets often do not provide parasitic values for high speed noise and propagation speed consideration.

Active devices, components such as integrated circuits, are often offered in several packages. In general, DIP packages, in either plastic or ceramic, have been the predominate package . These typically are the largest packages and provide the poorest high speed operating environment due to lead configuration. The next best package style is the Surface Mount Package. These are offered in a variety of packages such as SOIC's, PLCC's, PFQP's or TSOP's These packages will typically reduce the lead capacitance and inductance.

To obtain the optimum performance from the device, the die can be directly mounted to the substrate using either the Chip-on-Board (COB), Flip Chip, Tape Automated Bonding (TAB) or similar approach. These offer an optimum approach since they minimize lead capacitance/inductance.

3.2 Intraconnection

3.2.1 Connectors

Intraconnections are often troublesome in high speed application because a continuous signal environment is not provided. Most board to board connector systems are not designed for use in high performance applications and compromise the signal integrity of the system. Board to board connections often mismatch the characteristic impedance designed into the board themselves, causing signal degradation.

There are two primary approaches to reduce the signal discontinuity caused by intraconnect systems. The first approach is to provide a connector style such that the pinouts can be arranged to provide a good signal path. Non-differential signals must reference between the active signal line and the closest reference plane connection, either a voltage or ground plane. Non-differential signal conductors rely on controlled geometries and nearby reference plane for impedance control. Signal pin quality, reference pin quality and their location controls electrical performance. To optimize performance, reference pins must be added to reduce the sharing problems. Generally a 3:1 signal to reference (ground or voltage) pin ratio is sufficient.

The second approach is to modify the connector to minimize the discontinuity distance between boards. This can be achieved by shortening the pin length, or by adding reference ground plane within the connector.

Board mounted coaxial connectors are frequently used when only a few signal lines are connecting to a circuit board or where either signal isolation or signal integrity is critical.

3.2.2 Cables

Discrete coax connectors and cables are often used because they can couple high speed, high frequency signals to a circuit board with little signal degradation. When there are only a few critical signals to interconnect between boards, a coax cable will control signal propagation speed, crosstalk , induced noise with excellent impedance match, particularly at higher frequencies. Discrete coax wires have been used with discrete wire boards for unique, high speed applications up to 18 Ghz. An optical cable can also be used with discrete wired boards for high frequency signals.

3.3 Printed Board and Printed Board Assemblies

Component placement is a critical factor in the design of high-speed systems. The effects of unsuitable placement can be significant and include concerns in the following areas:

- Crosstalk Management
- Impedance Control
- Power Distribution
- Time Delays Between Circuits
- Thermal Management

3.3.1 Board Design

The number of signal layers in multilayer boards will be influenced by the density of interconnections within the board as well as the effect of crosstalk or coupling between signal lines. Crosstalk control can add layers or can require increased space between conductors decreasing the interconnect density.

Discrete wired boards will be influenced by the density of

interconnections within the board as well as the effect of crosstalk. The use of diagonal wire routing on the same wiring layers as X and Y layers may allow greater circuit density per layer plus the placement geometries available can accommodate high density and low crosstalk.

A close relationship between design and performance exists in the case of interconnection lines involving high speed digital signals. This interdependence previously existed only in the very highest performance computers or could be ignored in low speed signal applications; however, due to increasing logic speeds, it now imposes new design rules, restrictions and process controls on products as ordinary as personal computers.

To meet the challenges of high speed digital processing, today's multilayer printed board must:

- reduce propagation delay
- manage transmission line reflectance
- reduce signal loss
- allow for high density interconnections

To achieve these desired goals the designer must start by controlling the impedance of the transmission lines which helps control reflectance when lines are effectively terminated.

Controlled conductors on boards can be used for signal interconnect between devices. For a given construction, impedance can be controlled with a specific dielectric thickness, conductor thickness, conductor width and the relative permittivity (dielectric constant).

Board material and its relative permittivity (ε_r) affects signal propagation and thickness for a given characteristic impedance as well as line width. Lower ε_r results in faster signal propagation, but increases conductor width for a given impedance value.

For discrete wired boards the conductor thickness and width is controlled by selection of the appropriate wire size. Since insulation on the discrete wires and the non-glass reinforced wire film can result in a lower "effective" relative permittivity for a given construction, the result is higher signal propagation speeds in discrete wire boards.

When designing to specific impedance values, material controls performance (as transmission lines) with measurable parameters such as the capacitance and the material between conductors. Signal paths should be kept short to minimize propagation delays. Even if it were possible to make a circuit capable of switching at infinite speed, the interconnection material would dictate the performance of the systems. Figure 1 illustrates the switching speed of a device vs propagation delay in a FR4 dielectric commonly used in the printed board industry.

Space constraints, number and complexity of interconnections, power distribution and cost of manufacture are some

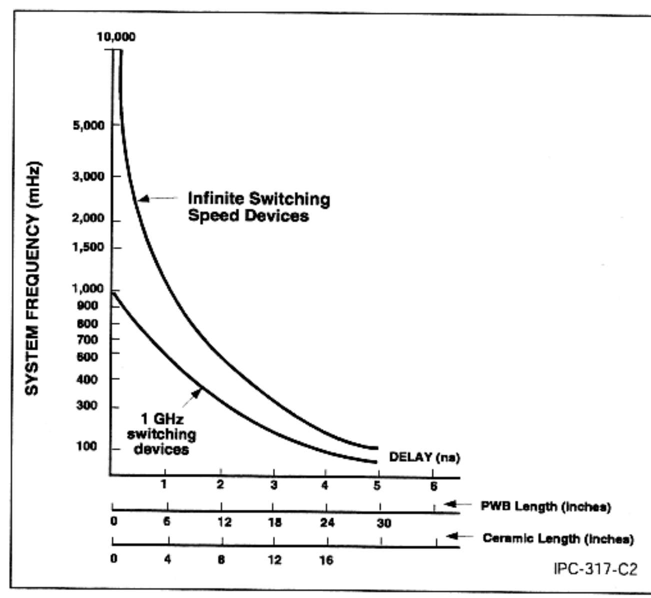


Figure 1 Switching Speed vs Propagation Delay

factors to be considered when determining the number of layers. The thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric, conductor width/thickness and the overall circuit length will impact performance. The width and thickness of the conductor and the number of layers have an effect on manufacturing costs.

3.4 Performance Requirements

Electromagnetic wave propagation theory must be considered in evaluating the performance of the interconnect and their substrates. High-speed devices are characterized by the short rise time of the pulses. As the rise time of the pulse decreases, the frequency content of the wave form increases and the circuit board looks increasingly like a high speed AC circuit.

3.4.1 Power Distribution

For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in electrical current from the power supply. If several devices demand current at the same instant, the power distribution system is required to meet these demands while maintaining its voltage. This requirement demands low inductance connections to devices with high supply capacitance for the various voltages in the system. At very high speeds, the impedance of the power supply is too high to supply the switching currents. As a result, the switching currents must be supplied by capacitors close to the drivers.

3.4.2 Relative Permittivity (Dielectric Constant)

The relative permittivity, ε_r, of a substance is defined as the ratio of the permittivity of the material to the permittivity of free space, which has a value of 1.00. Dielectric constant

is the term in common use in industry even though "dielectric constant" varies with several parameters. Factors that influence the relative permittivity of a given material include the electrical frequency at which the measurement is performed, temperature, and extent of water absorption. In addition, if the material is a composite e.g. a reinforced laminate, the value of ε_r may vary enormously as the relative amount of resin and glass of the composite is changed.

The relative permittivity (ε_r) of the dielectric of an interconnecting structure will affect electrical performance. The choice of ε_r is used in the design of the structure to meet the impedance, capacitance and propagation time requirements of the system. For a given conductor line geometry, propagation time will vary directly as the square root of ε_r, impedance inversely as the square root of ε_r, and capacitance directly as ε_r.

The effective relative permittivity, ε_r', is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. An experimental value of ε_r' may be obtained using a Time Domain Reflectometry (TDR) technique or by measuring propagation delay for a known length line and calculating a value.

3.4.3 Relative Permittivity and Frequency Relationship

Values of both ε_r and ε_r' are dependent on the reinforcement to resin ratio, temperature, water absorption and the frequency at which the measurement is performed. Steps should be taken to ensure that electrical measurements are performed under conditions that are similar to the final application.

Some materials, such as an FR-4 flame retardant epoxy/glass laminate, exhibit a dependence of frequency component of dielectric properties, and it becomes important to choose carefully the frequency at which measurements are made. Select the frequency such that the dielectric parameters obtained may be used to provide a precise prediction of the electrical characteristics of the finished printed board.

Since most performance characteristics of a printed board are determined by TDR measurements, it is appropriate that the frequency of these TDR measurements is the frequency of choice for comparing dielectric properties. The highest frequency of concern or bandwidth (BW) in Gigahertz of a digital pulse may be obtained from the relationship.

$$BW = 0.35/t_r$$

where, t_r in nanoseconds is the pulse rise time from 10% to 90% of its maximum value. Thus, a typical TDR pulse, with a rise time of 100 psec, has a bandwidth of 3.5 GHz. (Some degradation of this rise time, however, occurs in transmission through the test fixture, thus reducing the effective frequency somewhat.) This dictates that dielectric measurements made by methods other than TDR must be conducted at high frequency.

An equation to predict world wide average from North America, Europe and Far East suppliers, based on a large sample of FR-4 is:

$$\varepsilon_r = 4.97 - 0.257 \log f/10 \times 10^6$$

Figure 2 represents an average which takes that into account. Z_0 predictions will more closely agree with TDR measurements if a value of ε_r of 4.1 is used since TDR testing is done at very high frequencies. Three sigma variation was measured at ±0.35 (8%). Three sigma line to line ε_r variation on a PWB panel was measured at ±0.26 (6%). ε_r is related to the resin to glass ratio.

Figure 2 shows plots of the ε_r measured over the frequency range 100 kHz to 10 GHz, for an FR-4 type laminate with a glass-to-resin ratio of approximately 40:60 by weight. The value of ε_r for this laminate varies from about 4.7 to 4.0 over this frequency range. This change in the magnitude of ε_r is principally due to the frequency response of the resin and thus is reduced if the proportion of glass in the composite is increased. In addition, the frequency response will also be changed if an alternative resin system is selected. Material suppliers typically quote values of dielectric properties determined at 1 MHz.

3.4.4 Critical Signal Speed

The general rule is that transmission line effects (wave effects) become an important design consideration when the length of the interconnection (conductors and plated-through holes) approaches 1/7 of the wave length of the signal. If the system clock frequency is 300 MHz, the wavelength in air is about 1 m. Generally, the system clock is a repetition of a square wave pulse. In most digital systems, data is carried in the leading edge of the pulse (the sharp rise). This edge must be permitted to rise (or fall) as quickly as possible. Frequency and the rise time of the signal are related by the relation $t_r = 0.35/f$ where t_r is rise time in nsec and f is the frequency in Ghz. Unfortunately, high speed signals have frequencies in the 100 Mhz to 1 Ghz range. Successful controlled impedance design requires the use of ε_r in this range.

Table 1 shows the rise times for some families of the IC's.

For example, ECL has a 0.45 nsec rise time with a corresponding frequency of concern of 0.35/0.45 GHz or 777 MHz. Using the formula, $T_{pd} = \frac{\sqrt{\varepsilon_r}}{C}$, this translates to a wavelength in air of about 15″, 7.5″ in FR-4 or less than 4″ in ceramic. This means that for printed boards fabricated from FR-4, if the interconnection path is more than 10″, the electromagnetic properties of the signal, and transmission line effects should be considered.

Note: The critical signal speed is the signal rise/fall time of

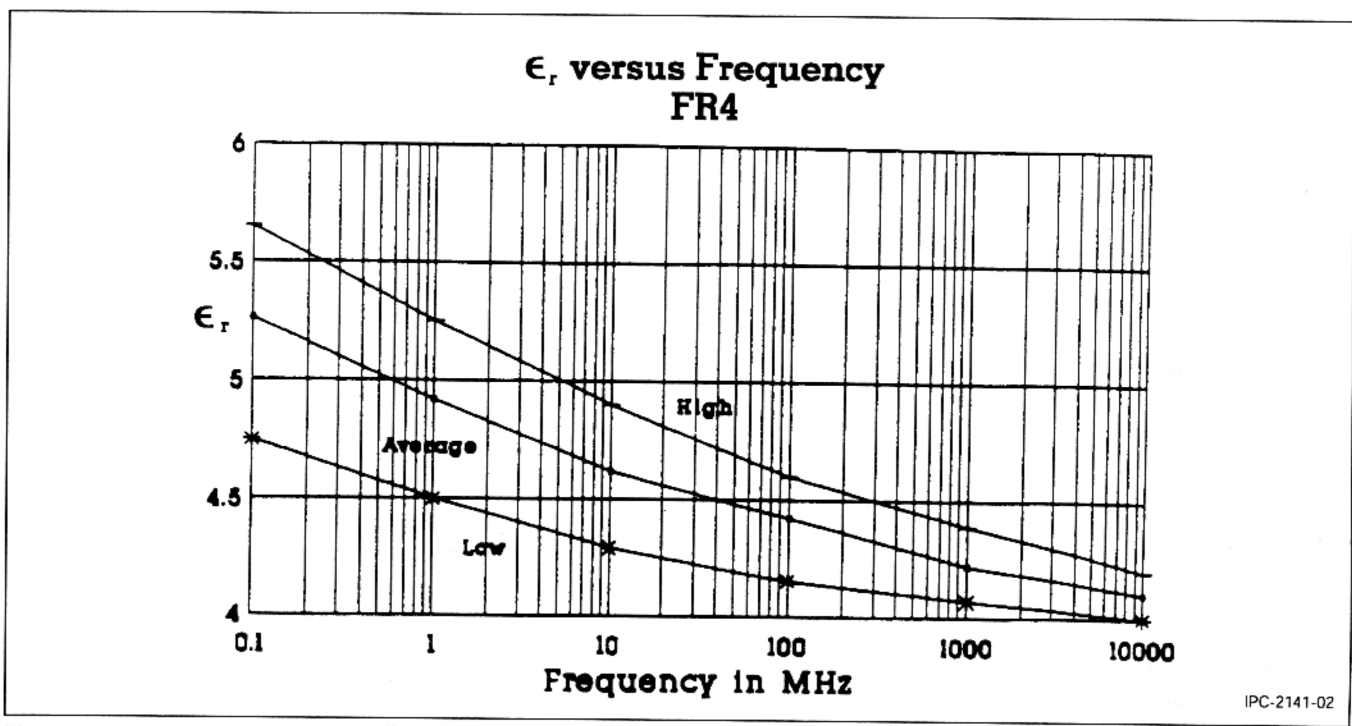


Figure 2 ε_r **Versus Frequency (FR4)**

Table 1 Device Rise Time

Device rise time	
Device family	**Rise time nanoseconds(nsec)**
TTL	6-9
Schottky TTL	2-3
ECL	0.45-0.75
GaAs	0.05-0.20

the device, not the clock frequency. This is a mistake often encountered in high speed logic design.

3.4.5 Capacitive Line Versus Controlled Impedance Line Environment

In high speed logic designs, conductor lines can either be treated as a transmission line or a capacitive line. For transmission lines the design concept is to provide a known characteristic impedance with a matching impedance to minimize reflections resulting from fast rise time pulses. For a capacitive line, the concept is a line whose stored charge requires a certain amount of current flow and results in changed voltage detected at the destination. The critical design parameters and requirements will depend on which concept is appropriate.

3.4.5.1 Capacitive Line

When the signal line is considered a capacitive line, the propagation time is calculated assuming the line plus the loads connected to it are purely capacitive. Because the reflections on the short interconnecting line occur several times during the pulse's rise time, the net result is a degradation of the edge transition time, i.e., slowing down, as opposed to distinct steps that occur in transmission lines.

3.4.5.2 Controlled Impedance Line

The characteristic impedance (Z_0) of the conductor follows Ohm's Law (R=V/I). For a high speed circuit, the critical difference is that the AC components of the circuit trace, the inductance and capacitance dominate the impedance equation, $Z_0 = R + \sqrt{\frac{L}{C}}$. The resistance, R, is a very small value and doesn't react to high speed or AC signals, but , L, the inductance and C, the capacitance do react. In simple terms, a capacitor passes AC and blocks DC, the reason they are used for AC coupling and decoupling (the AC component goes to ground). On the other hand, an inductor passes DC and blocks AC, useful for DC coupling of noisy power lines. Because of the relationship in the formula, increases in the capacitive component result in decreased impedance; increases in the inductive component result in increased impedance. As the frequency goes up, the effective impedance of an inductor goes up and as the frequency goes up, the effective impedance of a capacitor goes down. Inductance of etch is determined by the conductor while capacitance is determined by relative permittivity, spacing between the conductor and the reference plane and the conductor area.

Impedance is important in high speed PCB design for several reasons.

First, applying the definition above, the amount of current that the circuit element (driver) will need to drive a conductor depends on Z_0.

Second, in high speed systems with mismatch along the signal path, reflections will occur. Reflections not only reduce the amount of power reaching the receiver, but may also cause ringing (noise) along the circuit. These forms of signal degradation can cause systems to malfunction due to missing datapulses (from attenuation drop out) or spurious datapulses (from reflection noise).

The resistivity of the conductor, typically copper, does not contribute significantly to the high speed circuit impedance. Both of these effects are because the ratio of driving voltage to current (V/I = impedance) is determined before the signal reaches the end of the circuit.

3.4.6 Bandwidth

From Maxwell's equations, it can be shown that velocity for a signal through a transmission line :

$$1/v = \frac{\sqrt{\varepsilon_r}}{c}$$

where c = the speed of light
v = velocity

At low frequencies, a signal path on a circuit board may usually be represented electrically as a capacitance in parallel with a resistance. However, as the frequency is increased, this approach of lumped circuit modeling breaks down and signal paths must be regarded as transmission lines.

For controlled impedance conductor interconnection, the electrical and dielectric properties of the board materials have increased importance and greater care must be taken with the design and termination of the circuit. Several attempts have been made to define the point at which conductors act as transmission lines. The required analysis needs to be performed in either the frequency or the time domain. However, the critical point to remember for digital signals is that it is the pulse rise time, and not the rate at which the device is clocked, that is the key determining factor. The clock rate is a dependent parameter since the faster the rise time the faster a device can be clocked.

The point at which a printed board significantly affects the transmission characteristics of a propagating pulse, widely cited within the printed board community, compares the rise time to the path length. The premise is to determine, for the transmission of a pulse of a given rise time, the length of a conductor before a significant voltage difference is realized along its length. Conductors longer than this critical value are then regarded as transmission lines. If the maximum voltage drop is greater than half the pulse height value, the circuit is regarded as a transmission line. This length is important due to other practical considerations.

For longer path lengths, reflections from a mismatched load impedance may be received back at the source after the pulse has reached its maximum plateau value, and pulse additions that occur under these circumstances may lead to false triggering of a device. For shorter path lengths, reflected pulses are received back at the source before the pulse has reached its plateau value. Therefore, any modification of the pulse shape will only be to the leading edge, which is less likely to produce false device triggering. Values are listed in the 6th column of Table 2. It has been suggested that circuit conductors longer than 50% of the wave length be regarded as transmission lines allowing a greater margin in the design. Wavelength values are shown for various logic families in column 5, Table 2.

3.4.7 Propagation Time

For a system to perform correctly at high speeds, a controlled propagation time may be required. In some cases adjustments in the propagation time for certain nets may be required by controlling total etch length from source to load.

3.4.7.1 Propagation Delay Time

The propagation speed of an electromagnetic wave is related to the permittivity of the insulating medium by the relation, $V_p = \frac{c}{\sqrt{\varepsilon_r'}}$, where c is the velocity of light (3 x 10^8 m/sec) and ε_r' is the relative permittivity of the dielectric material. The relative permittivity and propagation times for various materials is shown in Table 3.

It may be seen that propagation delay time is directly proportional to the square root of the effective relative permittivity. In order to calculate the propagation time for a signal transmitted down a specific conductor, one must use the above equation and refer to section 3.4.2 if a value needs to be derived for ε_r' from known values of ε_r for the surrounding dielectrics. Alternatively, consult section 4.2 which lists a compilation of equations for several circuit configurations.

3.4.8 Signal Loading Effects

When a conductor is connected to several loads (devices), signal loading must be considered. When connected in serial fashion and the impedance of the load is low or a near match to the characteristic impedance of the line, there will be a decrease in signal amplitude as each load is reached. High impedance loads relative to the line will result in a smaller decrease in amplitude. A matched load at the end may be necessary to prevent a reflection that could send a false pulse (false triggering) on the line. The transmission line (controlled impedance) concept is usually appropriate.

Radial or star connections to loads may result in complex reflections from the open ends of each line adding to each other. This method of connecting should be avoided in high speed design.

Table 2 Typical data for some logic families

Logic Family	Rise Time nsecs	Bandwidth MHz	Wavelength In free space m	Wavelength In FR-4* m	Wavelength ½ Rise FR-4* m
TTL	8	44	6.8	3.1	0.55
Schottky	3	120	2.5	1.2	0.21
TTLECL	0.6	580	0.52	0.24	0.041
GaAs	0.1	3500	0.086	0.040	0.0069

*Relative permittivity of FR-4 was taken as 4.7

Table 3 Propagation time in various materials

MATERIAL	ε_r (at 30 MHz)	VELOCITY (IN/nSEC)	VELOCITY (pSEC/IN)
Air	1.0	11.76	84.9
PTFE/Glass	2.2	7.95	125.8
RO2800	2.9	6.95	143.9
CE/Custom ply	3.0	6.86	147.0
BT/Custom ply	3.3	6.50	154.0
CE/Glass	3.7	6.12	163.0
Silicon Dioxide	3.9	5.97	167.0
BT/Glass	4.0	5.88	170.0
Polyimide	4.1	5.82	172.0
FR-4/Glass	4.1	5.82	172.0
Glass Cloth	6.0	4.70	212.0
Alumina	9.0	3.90	256.0

CE = Cyanate Ester BT = Beta-Triazine PTFE = Teflon™

3.4.9 Crosstalk

Crosstalk is the transfer of energy (coupling) between conductors by mutual inductance and capacitance. The energy from the "source" conductor becomes superimposed on the "receptor" conductor, leading to spurious switching and circuit dropouts. Signals introduced into the active line will be induced into the quiet or passive line by electromagnetic fields that accompany the traveling signal on the active line. The near end refers to the signal originating end, and the far end, the signal receiving end.

The coupled signals traveling toward the far end are called forward crosstalk and the coupled signals in the passive line coming back to the near end are called backward crosstalk.

The coupling due to capacitive effects causes a low level replica of the active signal to be sent to both the far and the near ends, with the same polarity as the active signal.

The coupling due to the inductive effects also sends signals to both the near and the far ends, but the signal to the far end is inverted (opposite polarity) to that of the active signal. Consequently. the backward crosstalk component of the inductive and capacitive coupling is the sum of the signals, but the forward crosstalk component is the difference between the two signals, usually resulting in a smaller crosstalk component.. Backwards crosstalk reaches a maximum in short parallel runs and is of most concern.

The crosstalk coupling coefficients found in references differentiate between the forward and backward coefficients.

The level of the transferred (coupled) signal decreases with shorter parallel line segments, wider line separations, thinner dielectrics, and longer pulse rise times. Conductors that are parallel for long lengths either on the same signal plane or on adjacent signal planes are susceptible to induced crosstalk. A victim line can also run parallel for short distances to several other lines. If a certain combination and timing of pulses on the other lines occurs, it can induce a signal on the victim line. Thus, there are requirements that the crosstalk between lines be kept below some level.

Typically, crosstalk is a concern when high-speed devices are used because of the fast rise time. Mixing logic families also causes concern because of the mixture of various voltage swings, noise margins and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL swings 3 volts and the ECL family has only a 100 mV DC noise margin, significant undesired coupling can occur.

3.4.10 Signal Attenuation

High-speed systems generate short rise time pulses and may respond ambiguously to pulses exceeding maximum rise time. Signal attenuation increases rise time and

decreases the amplitude of the pulse. This is best explained in terms of the model of a pulse as a sum of signals of several frequencies. The high frequency components of the pulse attenuate more rapidly than lower frequency components. This is due to the skin effect in the conductor as well as the dissipation effect in the dielectric.

Signals may be further attenuated by the resistance of the copper used in the conductor and by skin effect losses resulting from the finish of the copper surface.

The resistance of the copper may reduce the steady state voltage levels below the levels needed for adequate noise immunity. This is especially true of ECL circuits where a voltage divider is formed by the terminating resistor and the line resistance.

DC resistance can be calculated using the copper resistivity and the geometries of the conductors being used. The skin effect can also be determined by formula and is a function of frequency. At higher frequencies, the current does not penetrate the conductor, so the need for thick conductors may not be necessary.

3.4.11 Termination of Nets

Termination of nets may be necessary to satisfy signal integrity, timing, voltage requirements of drivers and receivers and impedance matching. Terminations prevent reflections by absorbing the energy. Common termination types are detailed in the following paragraphs and as shown in Figure 3.

Series resistor terminations are the use of a resistor in series between the driver and the line, used most commonly to match the net to the driver impedance. A series termination controls overshoot, requires only one component and consumes little power, but can effect rise time/fall time. To be most effective series resistor must be placed close to the driver.

Shunt terminations connect the end of a net to the ground. A serial chain load with a driver is a typical application. The terminated resistor must match the value of the net impedance and will have low reflections. This configuration provides for easy routing of distributed loads and provides no delay degradation.

Thevinin terminations are resistor dividers usually connected to voltage and ground at the end of the net. There is no delay degradation and a defined DC bias is established by the choice of resistor values, and incident switching occurs at the load. This termination consumes more power, requires two components and has effects on DC offsets for high and low logic states.

Resistor capacitor terminations, called AC terminators, are placed at the load end of the net, usually ground. They control overshoot and spiking, consume no dc power, and smooth edges of wave forms. The value of the resistor is Z_0 and capacitor value must be chosen to appear as a short circuit at the edge rate frequency.

A diode clamp termination can be either pulled up by V_{cc}, pulled to ground, or both. The effect is to clamp overshoot and undershoot. Diode clamps do not terminate nets. They are the more expensive solution to a reflection problem.

3.4.12 Additional Signal Integrity Issues

In addition to the above signal integrity issues, other effects may have to be considered in high speed/high frequency design. Some of these are skew, overshoot, ring back, threshold violations and coupling due to simultaneous switching.

3.4.12.1 Skew

Skew is the effect of signal that needs to arrive at the same time being delayed with respect to another due to different path lengths delay that may cause timing errors in the design. As an example, clocks and their relationship to selected devices using clock signal may be affected by skew. Skew can be affected by conductor impedance, differing conductor lengths, power supply variation, device tolerances and load capacitance of inputs.

3.4.12.2 Reflections

Overshoot is the effect of excessive voltage above V_{cc} or the complement, excessive voltage below ground, undershoot. Components have greater or lesser tolerance to voltage and the designs should meet the component data sheet requirements. Overshoot can be controlled by different schemes external to the devices by some of the termination methods discussed elsewhere.

3.4.12.3 Ring Back

Ring back is the effect of the rising edge of a logic transition, meeting or exceeding the logic, then recrossing the threshold before settling. This can be caused by mismatch of logic drivers and receivers, poor termination techniques and impedance mismatch of the net to the devices.

3.4.12.4 Threshold

Threshold violations are caused when a rising pulse edge does not reach the voltage threshold of the device input. Weak drivers or poor terminations are often the cause although it can also be caused by device drivers with a large rise time versus pulse width.

3.4.12.5 V_{cc}/Ground Bounce

Simultaneous switched outputs may be inductively coupled between V_{cc} and ground. This delays transition and may change rise and fall times. Without an accurate model of the V_{cc} and ground and package models, accurate simulation is difficult. Provision for low inductance connections using wider conductors helps to reduce the inductive effects.

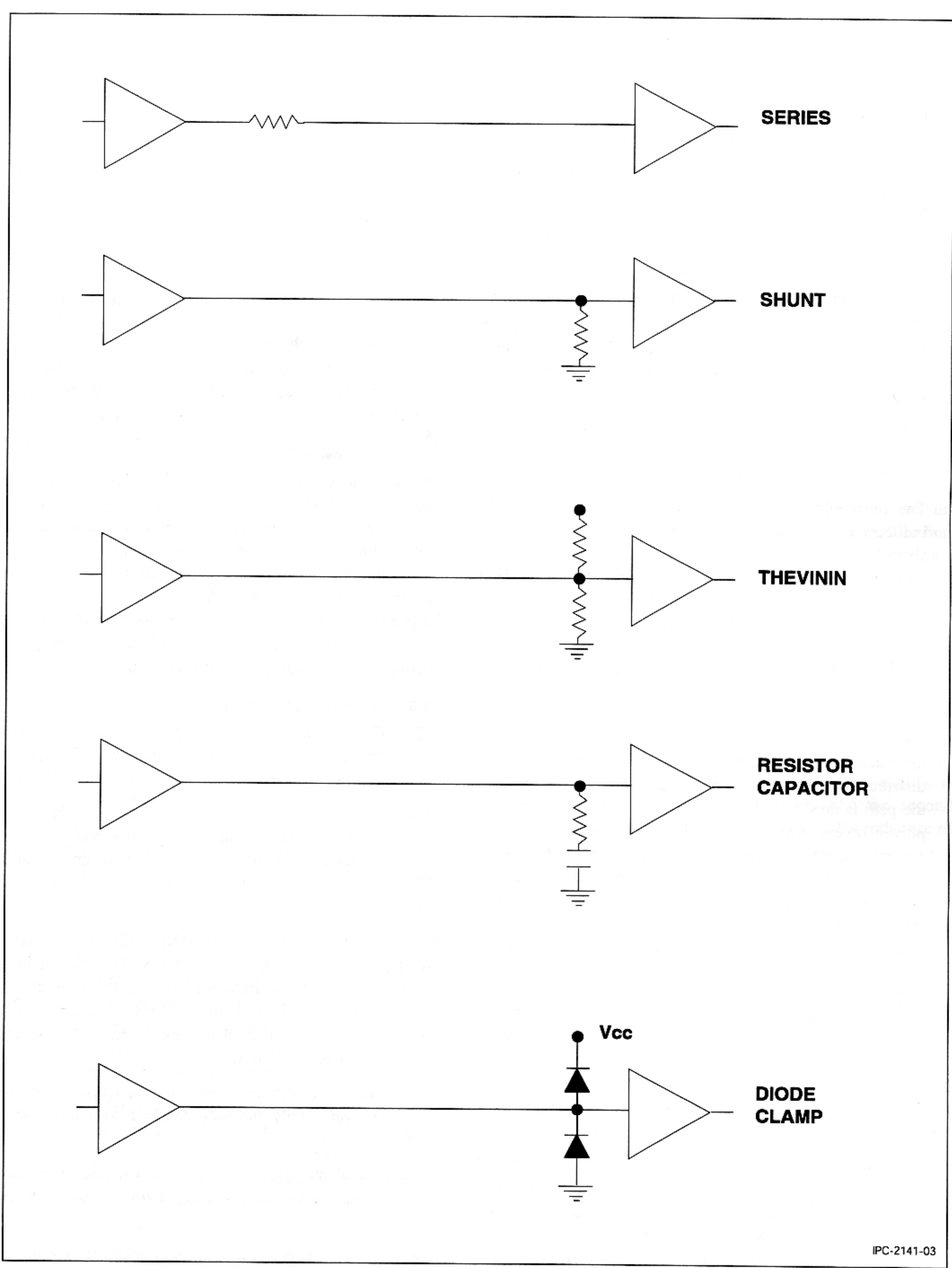


Figure 3 Termination of Nets

3.4.13 Switching Noise

When devices are switching, current is either drawn from or passed to the power supply through the power/ground paths. When this current has high frequency components, the self inductance of the leads and traces become significant, leading to transient or switching noise.

These transients are caused by the inductance of the power/ground loop and the layout must be designed to reduce this inductance as much as possible.

A common technique to reduce switching noise is the use of decoupling capacitors that serve to provide the current from a point closer to the IC than the power supply. When this is done, the positioning of the capacitor is important. If the capacitor leads are too long, the self inductance becomes too high and unwanted switching of adjacent circuits occur.

The decoupling on boards is normally achieved with discrete capacitors that can be closely positioned to the device with short power and ground terminations.

The most effective way to minimize the effects of lead inductance is to choose component packages with very short leads and then to connect them into the power and ground planes with the shortest possible path. The best technique is to use a via at the component land connected directly to the power or ground planes.

3.4.14 Other Parasitics Noise

Multilayer boards have advantages over double sided boards in that the power/ground planes are continuous layers of metallization. Consequently, they offer a lower RF impedance to the spurious currents and improved current distribution. The current loop is significantly reduced since the path is now bounded by the signal wire length and the power layers. For further improvements in multilayer designs, adjacent layers (signal) can be run orthogonally thus reducing the crosstalk due to the small crossover area between conductors. The power and ground layers will also serve to isolate noisy signal conductors by shielding emissions with a continuous metal plane.

3.4.15 Noise Budget/Noise Margin

A noise budget is defined as allowance for a voltage change of the system DC and AC voltage that allows a device to operate within specific limits. There are two primary components of the noise budgets. The first is the DC power supply noise of each integrated circuit. and the second is the device logic signal AC noise budget.

Each logic device connects to a voltage and a ground return. The system power distribution has finite AC and DC voltage drops between the power supply and component. Also the power supply has a designated operating tolerance. The primary parameters that are included for the noise margin are:

a) Power supply variation

b) Reflections

c) Ground bounce

d) Ground offsets

e) Thermal offsets

f) Crosstalk

g) Ground IR drop

h) Reference accuracy

I) Terminator noise

Erosion of the noise budget also includes reflections, coupling noise, and ground bounce in the power leads.

3.5 Power Distribution

The DC and AC characteristics for degrading power distribution may be grouped into two major categories, conductive losses (DC) and dielectric (AC) losses.

3.5.1 DC Power Distribution

Power distribution system (DC) encompasses the output of the power supply to the input of each device. For systems with many circuit boards and supplies, a simulation of the interaction of each component is desirable to verify and assist the design effort. The voltage drop between any two points on a copper plane, is determined by multiplying the maximum load current by the plane sheet resistance. When necessary, model analysis is used to determine voltage drop between each integrated circuit location.

3.5.2 AC power Distribution

The AC power distribution is divided into three contributing elements of impedance. Since this is an AC signal, it is considered as a power distribution impedance network.

The first is the switching transient impedance. This impedance is between the decoupling capacitor and lead of the device. This element is also referred to as ground and/or Vcc bounce. This is the highest frequency component of the current.

The second element is the impedance due to the charging of the bulk IC decoupling capacitors. The current in this impedance is at lower frequency and higher amplitude than the current in the first element. The voltage drop will be less than the above due to the lower impedance resulting from the lower frequency.

This current that recharges the bulk capacitors is provided by the power supply and will usually have the lowest frequency element.

The third element is the decoupling capacitor impedance created when the decoupling capacitors supply current to the ICs.

Decoupling must provide sufficient current for the devices. This includes high peak current requirements during device

switching. The circuit board power system must provide this current without lowering the supply voltage below the required minimum device level. When the stored energy on the board is insufficient, capacitors are placed near the devices, connected between the power and ground planes to provide this current. The capacitors provide the charge current to the device instead of the power planes. When they discharge their current into the device they quickly recharge from energy stored in slower discharging capacitors in time for the next discharge.

4.0 Design of Controlled Impedance Circuits

In high-speed design there are many considerations. It is the job of the circuit designer to understand the system specifications and weigh the alternatives to provide the simplest, cost effective, reliable solution for meeting those specifications, including the selection of the best printed wiring or discrete wiring board features. In cases where high speed signals are present, the signal conductors may need to be considered as transmission lines. This means, as a minimum, specifying the characteristic impedance of those lines. Since transmission lines should be terminated in their own impedance, a designer may also provide for termination.

The tolerance and value of termination resistors must be chosen to match the conductor and design requirements. The following should be considered:

a) Termination for each signal line increases density and complexity.

b) Placement should be made so that signals travel the shortest path from source (driver) to load (termination).

c) Circuit board technology must be capable of controlling impedance.

d) Minimum component to component spacing may eliminate the need for controlled impedance lines but may increase etch density.

Placing high-speed components close together might reduce the need for transmission line parameters and reduce crosstalk problems. This may also result in thermal management problems and increase the number of layers in a printed board due to increased density. Increasing the spacing will reduce the thermal problems but could add crosstalk and impedance restrictions.

Circuit impedance is important in board design for several reasons. The amount of current that a circuit element (driver) will need to conduct a signal path depends upon Z_0. This is taken into account in the design of IC's and can affect how receivers may be placed along the circuit. (see section 3.4.8 on signal loading effects).

Furthermore, in high-speed systems, any mismatch along the path that a signal must travel will cause reflections. Reflections not only reduce the amount of power reaching the receiver, but also may cause ringing along the circuit.

Because the time period for measurement is very short, circuit termination does not offset the characteristic impedance. Likewise, the resistivity of the conductor material (typically copper) does not contribute significantly to the high speed circuit impedance. Both of these effects are because the ratio of driving voltage to current flow (V/I = impedance) is established before the signal reaches the end of the circuit.

4.1 Unbalanced Line Configurations

A microstrip line consists of a line separated from an "infinite" reference plane , at least 100 times the width of the etched line, by a layer of dielectric. In the simplest case, the conductor is on the surface of an outer layer where the conductor is surrounded by air ($\varepsilon_r = 1.0$) on the top and edges and on the bottom by a solid dielectric.

A special case of the microstrip is the embedded microstrip line where the line is buried some distance beneath the surface of the board, surrounded by solid dielectric. The buried microstrip has a single reference plane separated by a layer of dielectric. One case of the buried microstrip is where outer layer circuitry is covered by soldermask material on layer 1. The discrete wire board is another example of an embedded microstrip construction. The discrete wire is embedded in a dielectric and encapsulated by additional solid dielectric.

A stripline is a line that is embedded in solid dielectric between two "infinite" reference planes. There are two variations of this configuration, one where the stripline is centered between the reference planes and the second where the striplines are not centered so that the influence of the reference planes is not equal, but proportional to the distances. Discrete wire boards are often constructed in stripline configurations where one or more wiring layers are embedded in solid dielectric between two "infinite" reference planes.

Designs for controlled capacitance and impedance use calculations that can predict the capacitance of a conductor as well as the impedance. The equations are based on empirical work and are unique for different configurations.

4.2 Unbalanced Line Equations

Z_0 is the impedance, measured in Ohms. C_0 is the capacitance per unit length. Configurations are shown in Figure 4.

Note: Limitations of the formulas (range of accuracy) are shown in IPC-D-317.

Note: Use proper value for ε_r for the material and frequency used.

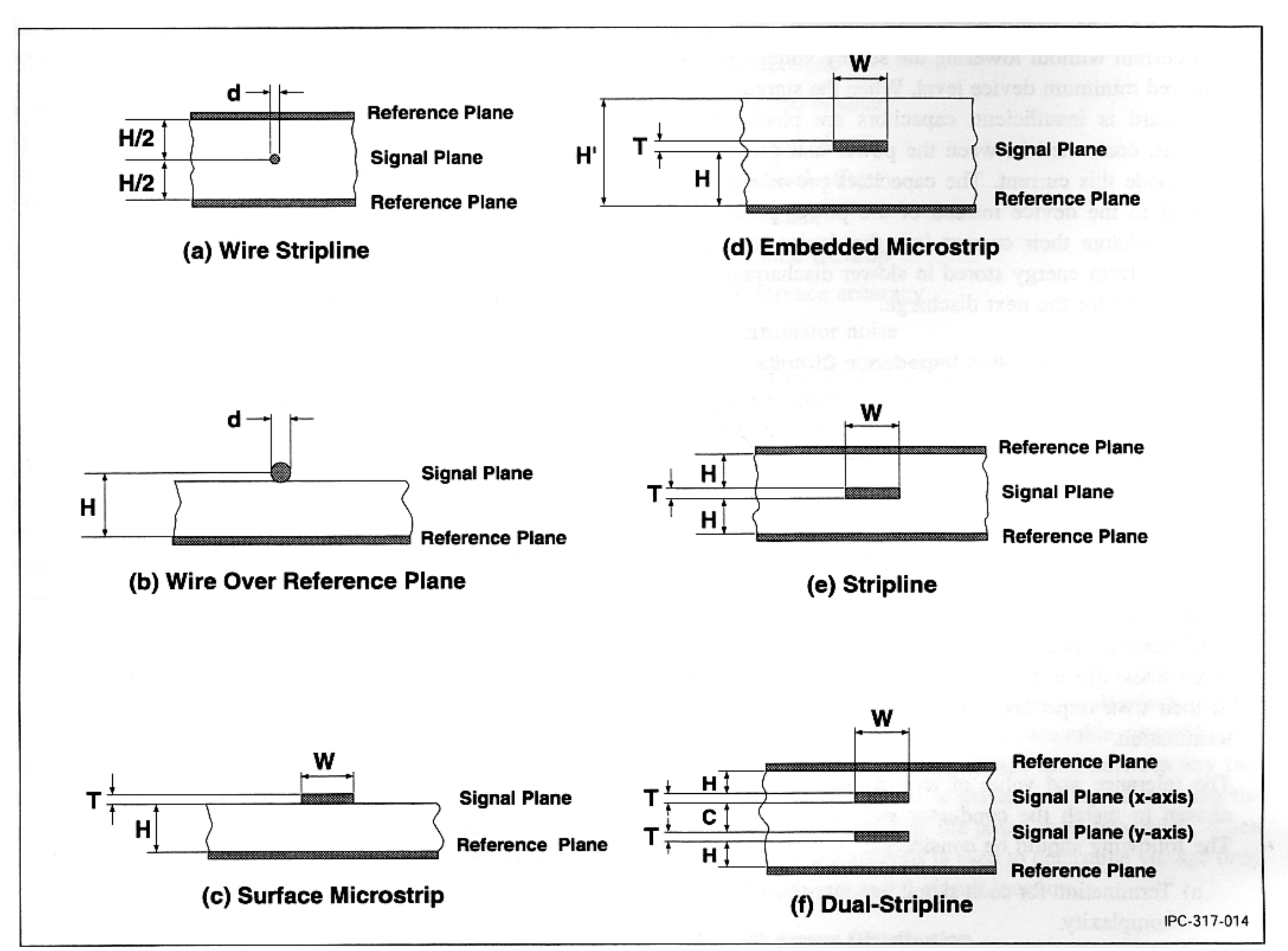


Figure 4 Typical Unbalanced Line Configurations

4.2.1 Surface Microstrip, Figure 4c

$$Z_0 = \frac{87 \cdot ln[5.98H/(0.8W+T)]}{\sqrt{\varepsilon_r + 1.41}} \text{ in ohms}$$

$$C_0 = \frac{0.67(\varepsilon_r + 1.41)}{ln[5.98H/(0.8W+T)]} \text{ in pF/in}$$

W is the line width
T is the line thickness
H is the dielectric separation between line and reference plane
ε_r is the relative permittivity
pF is picoFarads

4.2.2 Embedded Microstrip, Figure 4d

$$Z_0 = \frac{87 \cdot ln[(5.98H)/(0.8W+T)]}{\sqrt{\varepsilon_r' + 1.41}} \text{ in ohms}$$

$$C_0 = \frac{[1/(H+T)/ln(1-0.6897(\varepsilon_r + 1.41)]}{\sqrt{\varepsilon_r}} \text{ in pF/in}$$

W is the line width
T is the line thickness
H is the dielectric separation between line and reference plane
pF is picoFarads
H' is the distance between the air surface of the dielectric and the reference plane
ε_r' is the relative permittivity defined as

$$\varepsilon_r' = \varepsilon_r\left(1 + e\left(\frac{-1.55H'}{H}\right)\right)$$

4.2.3 Symmetric Stripline, Figure 4e

$$Z_0 = \frac{60ln[1.9(2H+T)/(0.8W+T)]}{\sqrt{\varepsilon_r}} \text{ in ohms}$$

$$C_0 = \frac{1.41(\varepsilon_r)}{ln[3.81H/(0.8W+T)]} \text{ in pF/in}$$

W is the line width
T is the line thickness
H is the dielectric separation between reference planes
ε_r is the relative permittivity

4.2.4 Dual (Asymmetric) Stripline, Figure 4f

$$Z_0 = \frac{80 \cdot ln[1.9(2H+T)/(0.8W+T)] \cdot [1-H/4(H+C+T)]}{\sqrt{\varepsilon_r}} \text{ in ohms}$$

$$C_0 = \frac{2.82 \cdot \varepsilon_r}{ln[2H-T/(0.268W+0.335T]} \text{ in pF/in}$$

W is the line width
T is the line thickness
C is the dielectric separation between signal layers
H is the dielectric separation between signal and reference planes
ε_r is the relative permittivity

4.2.5 Wire Stripline, Figure 4a

$$Z_0 = \frac{138}{\sqrt{\varepsilon_r}} ln\left(\frac{4H}{\pi d}\right) \text{ in ohms}$$

d is the wire diameter
H is the dielectric separation between reference planes
ε_r is the relative permittivity

4.2.6 Wire Microstrip, Figure 4b

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} ln\left(\frac{4H}{d}\right) \text{ in ohms}$$

d is the wire diameter
H is the dielectric separation between reference plane and wire
ε_r is the relative permittivity

4.3 Balanced Line Configuration

High performance digital systems can use differential signal connection configurations to provide better noise immunity and improved timing. The differential configuration, also called a balanced line, has different controlled impedance calculations and measurement techniques from the more common unbalanced line. The differences are detailed below.

A single ended conductor is the most common way to make connections between two devices. A single conductor connects the source of one device to the load of another device as shown in Figure 5. If these are high speed devices, the conductor should be a controlled impedance interconnection. Unbalanced transmission lines have one signal conductor and a common return path, usually a power or ground plane. Since the signal conductor cross-section is different than the return (plane) conductor, this case is called an unbalanced line. This can be a coax line, an unshielded twisted pair, or a printed circuit board in either a microstrip or stripline. Figure 6 shows some typical configurations.

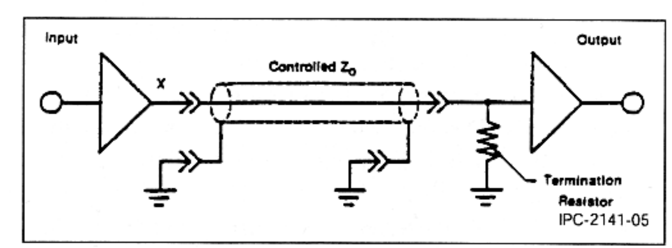


Figure 5 Unbalanced Line Schematic

The differential interconnect configuration is shown in Figure 7. The true signal and its logical complement are connected to the load. High speed devices are usually controlled impedance connections. This can be done with twisted pair with a shield, a coax pair or by pairs of conductors in the circuit with a reference plane as shown in Figure 8. Balanced lines are most often used to transmit differential signals. A balanced transmission line has two signal conductors usually accompanied by a reference plane or a cable shield. The geometrical and electrical relationship between each signal conductor and the common reference is the same and this is called a balanced line.

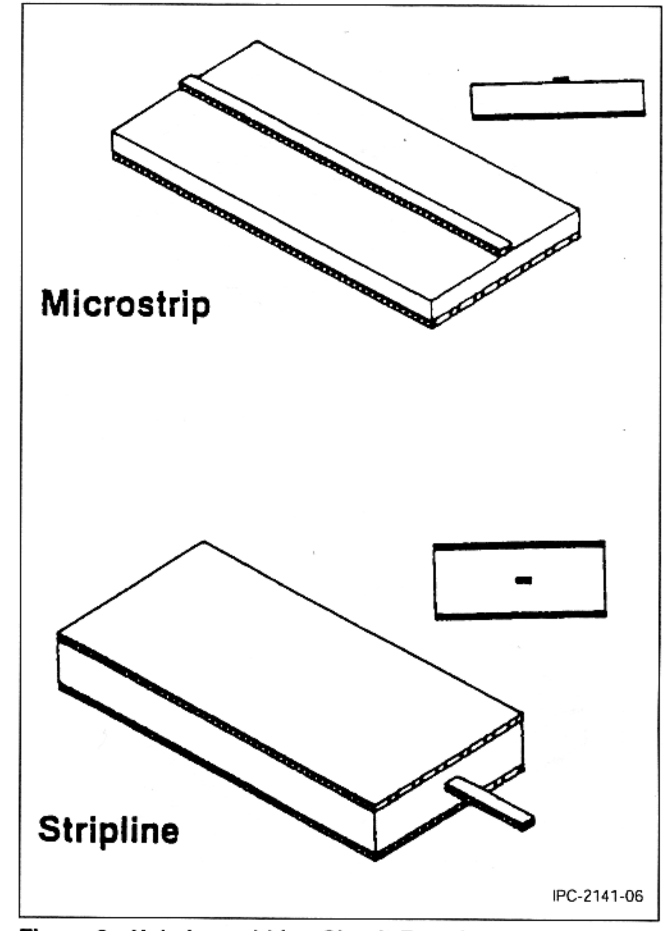


Figure 6 Unbalanced Line Circuit Boards

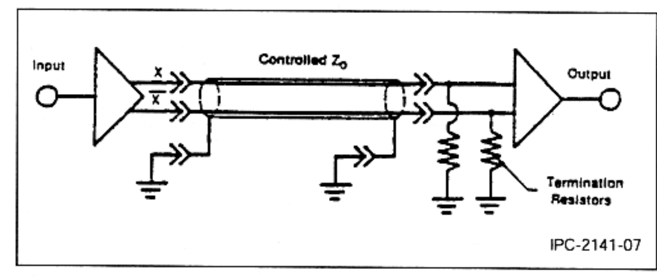


Figure 7 Balanced Line Diagram

There are advantages to the differential method. If the complementary conductors are close proximity to each other, then the signals will be switching directly opposite to

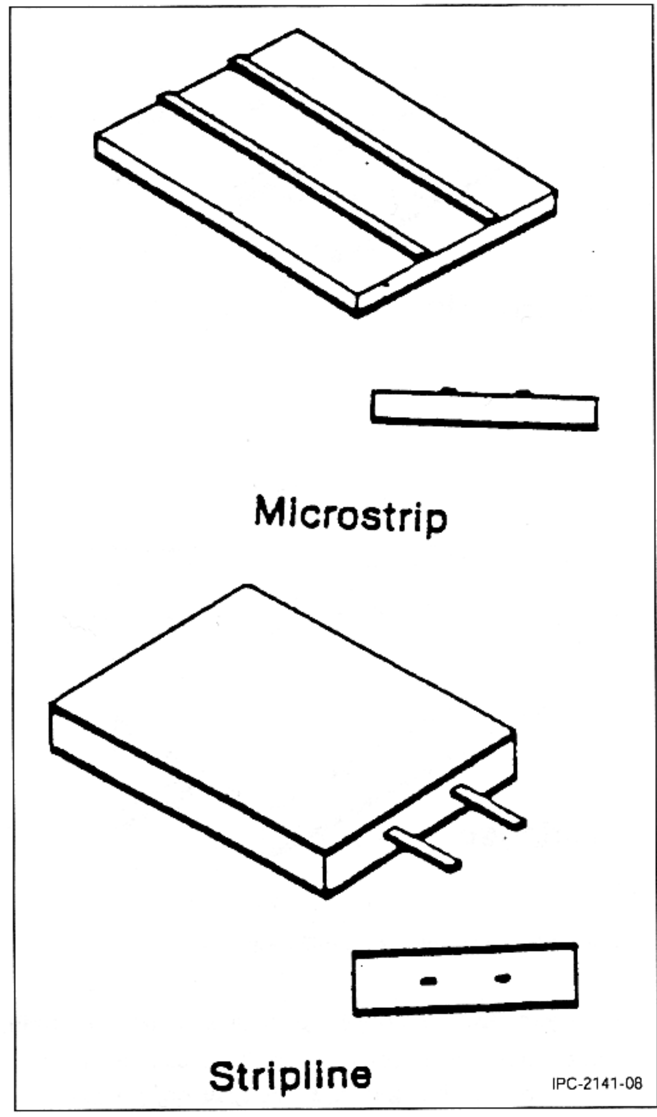


Figure 8 Balanced Line Circuit Board

each other and the fields generated will cancel each other reducing EMI and RFI. Additionally, any external noise will be sensed equally by both conductors. Because the receiver is seeing the differential voltage between the two conductors, the common mode noise is ignored by the receiver. The disadvantage is that two interconnect paths are required. For each conductor, they must be matched for impedance and time delay (length). ECL devices have true and complementary output, but CMOS and TTL logic do not.

The three configurations, surface microstrip, embedded microstrip, and symmetric stripline are shown in Figure 9 and the equations in the following section. It is strongly recommended that manufacturers empirically verify results by characterizing their own process as all equations are based on a model which may not practically represent the circuit behavior under every circumstance.

Testing and test configuration of differential conductors is covered in section 9.2.1.8.

4.4 Balanced Line Equations

Z_0 is the impedance in Ohms. C_0 is the capacitance per unit length. Configuations are shown in Figure 9. The specific formulas for calculating Z_0 and C_0 of the balanced line configurations exist in various forms, some of them in conflict. Research is currently underway to resolve these differences by means of both mathematical study and sample verification. Contact the IPC for current status of this effort.

4.4.1 Surface Microstrip

$Z_0 = f(\varepsilon, W, H, T, S)$
$C_0 = f(\varepsilon, W, H, T, S)$

4.4.2 Embedded Microstrip

$Z_0 = f(\varepsilon, W, H, T, S)$
$C_0 = f(\varepsilon, W, H, T, S)$

4.4.3 Symmetric Stripline

$Z_0 = f(\varepsilon, W, H, T, S)$
$C_0 = f(\varepsilon, W, H, T, S)$

4.5 Controlled Impedance Design Rules

When considering a controlled impedance/high speed design, the components and external I/O cables often dictate the values of controlled impedance required by the design. For instance if coax cable is the interconnect, standard cable impedance values are 50, 75, and 93 ohms. The board conductors should match these values. Impedance values of components are often in the 50 to 85 ohm range, dictating those values for the conductors. The range of values for conductors is generally in the 0.12 to 0.30 mm range which narrows the choices for the design even further. Dielectric thicknesses also restrict the choices for the physical design. The range of relative permittivity, shown in Table 3, are in a fairly narrow range as well, 2.9. to 4.5. Although more exotic materials may be used in very high frequency applications, economics dictate use of more conventional material for the bulk of the applications.

Power to drive a given impedance, noise, propagation and EMI sensitivity/radiation must also be considered as a part of the total solution of the design.

High impedance values in the board require fine lines and/or thick dielectric and practical limits are quickly reached (.1mm lines/.5mm dielectric, etc.) for printed circuit boards. Discrete wire boards offer an alternative to accomplish high density interconnects with high impedance within practical board physical constraints. The uniform (±2.5 μm) discrete wire also provides consistent impedance values throughout the signal length and over the entire board area.

Caution: Discrete wiring technology has a limited source and may restrict larger volumes.

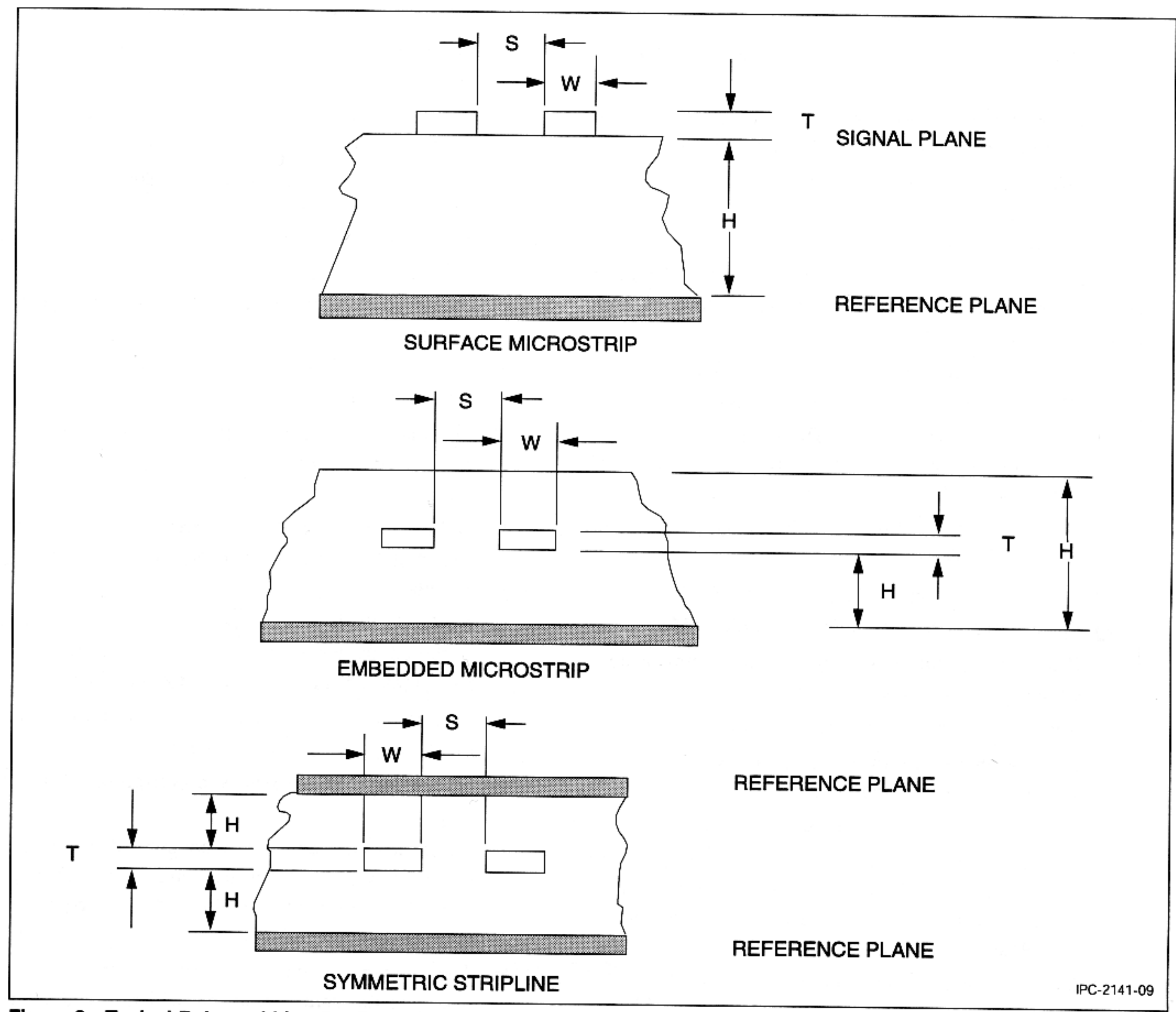


Figure 9 Typical Balanced Line Configuration

Required line impedance can be achieved as a function of the interaction of several parameters:

a) Conductor Cross Section - Conductors, particularly on outer layers, are sensitive to width due to plating and etching. Wider lines lower impedance while narrower lines raise it.

b) Type of line - For a given equal ε_r, spacing, and conductor width, impedance values will be greater for a microstrip than for a stripline.

c) ε_r, Relative permittivity - Higher ε_r results in a lower impedance value while increasing propagation time.

d) Dielectric thickness between signal and ground — lower impedance as thickness decreases.

Other factors to consider include:

a) Use thinnest copper allowable consistent with other design requirements. Impedance values decrease as the copper thickness increases.

b) Keep controlled impedance conductors at least 2.5 mm from the edge of the reference plane.

c) Avoid placing conductors over copper void areas greater than 5.0 mm square.

d) Route critical conductors on inner layers between reference planes or buried outer layers.

e) Avoid "extreme" builds such as fine conductors or thick board construction.

f) Place test control coupons in the circuit area or use active conductors with adjacent reference points (2.5 mm) as the test coupon.

g) Supply data for artwork in digital form, not plotted film.

h) Use different conductor codes for each controlled

impedance value on each signal layer.

i) Allow for solder mask in surface microstripline design.

j) Allow for widest tolerances for each dimension and parameters, in order to meet specified tolerances.

k) Give the fabricator latitude to vary construction.

4.6 Crosstalk Rules

Several rules can be used to control crosstalk. The most common techniques of reducing crosstalk effects in high density circuits are as follows:

a) Group logic families geographically. Restrict signal conductors for each logic family to those areas.

b) Place components away from I/O connector in descending order of speed, use short conductor runs to high speed I/O.

c) Terminate controlled impedance conductors to reduce reflections.

d) Limit use and length of parallel conductors.

e) Specify and control conductor to conductor spacing.

f) Place components close together to minimize conductor lengths and parallelism.

g) Reduce the signal to ground separation.

h) Isolate signal layers from each other by interspersing with power and ground layers.

i) Route adjacent signal layers orthogonally.

j) Isolate noise emitters such as clocks, high speed communications I/O and high speed bus interconnect on separate layers with power/ground separators or in isolated area of the board.

k) Increase conductor separation.

l) Reduce the line impedance.

m) Reduce the signal level.

4.6.1 Crosstalk Implementation

The impact on circuit board design due to implementation of the crosstalk rules will include:

a) Multiple power and ground planes are required.

b) Added complexity due to dense component placement.

c) Selective signal routing criteria.

These can greatly increase complexity and place limitations on the available circuit board technology.

In general, a board is populated as densely as possible with chip devices to minimize the size of the board and reduce propagation time. The result is that conductors run close to each other and usually the designer must resort to multilayer or discrete boards to handle the high interconnect density and the crossovers in the wiring plan.

4.7 Controlled Impedance Coupon Design Rules

The following are rules for designing the test coupon shown in Figure 10:

a) Use the same line width, copper weight, dielectric thickness, and dielectric type as the board.

b) Have a continuous power/ground under the conductor. Reference planes (power/ground) shall be continuous without breaks, voids, splits or interruptions of foil in the coupon area.

c) Locate coupons where they represent average plating, lamination, and etching conditions.

d) Use the same soldermask requirements for the board and the coupon.

e) No conductive material allowed within 2.5 mm of the test coupon (other conductors, copper robbers, etc).

f) Reference planes are to be interconnected in the coupon area and must be isolated from the rest of the circuit area.

g) All layers shall be identified on layer 1 at each end of the conductor. Conductive nomenclature shall be more than 2.5 mm away from test conductors.

h) Non-conductive nomenclature is permitted within the coupon area.

i) Square lands shall identify power/ground reference points.

l) Controlled impedance test coupons that cannot be designed within the finished circuit area shall provide sufficient area for vendor code, date code, serial number and part number.

m) The clearance from the controlled impedance conductor to the pattern shall be 0.25 mm and the pattern length shall be 2.5 mm.

n) The minimum controlled impedance conductor length between the two test points shall be 150 mm.

o) When two etch conductors are parallel on the same layer of the test coupon, the minimum center to center spacing between them shall be 0.5 mm.

p) There shall be test points and reference points, plated-through holes and lands, at each end of the test line.

Figure 11 shows a preferred test probe pattern for controlled impedance conductor testing.

4.8 Decoupling/Capacitor Rules

4.8.1 Decoupling Capacitance

Decoupling capacitors provide current to devices until the power supply can respond. High frequency switching,

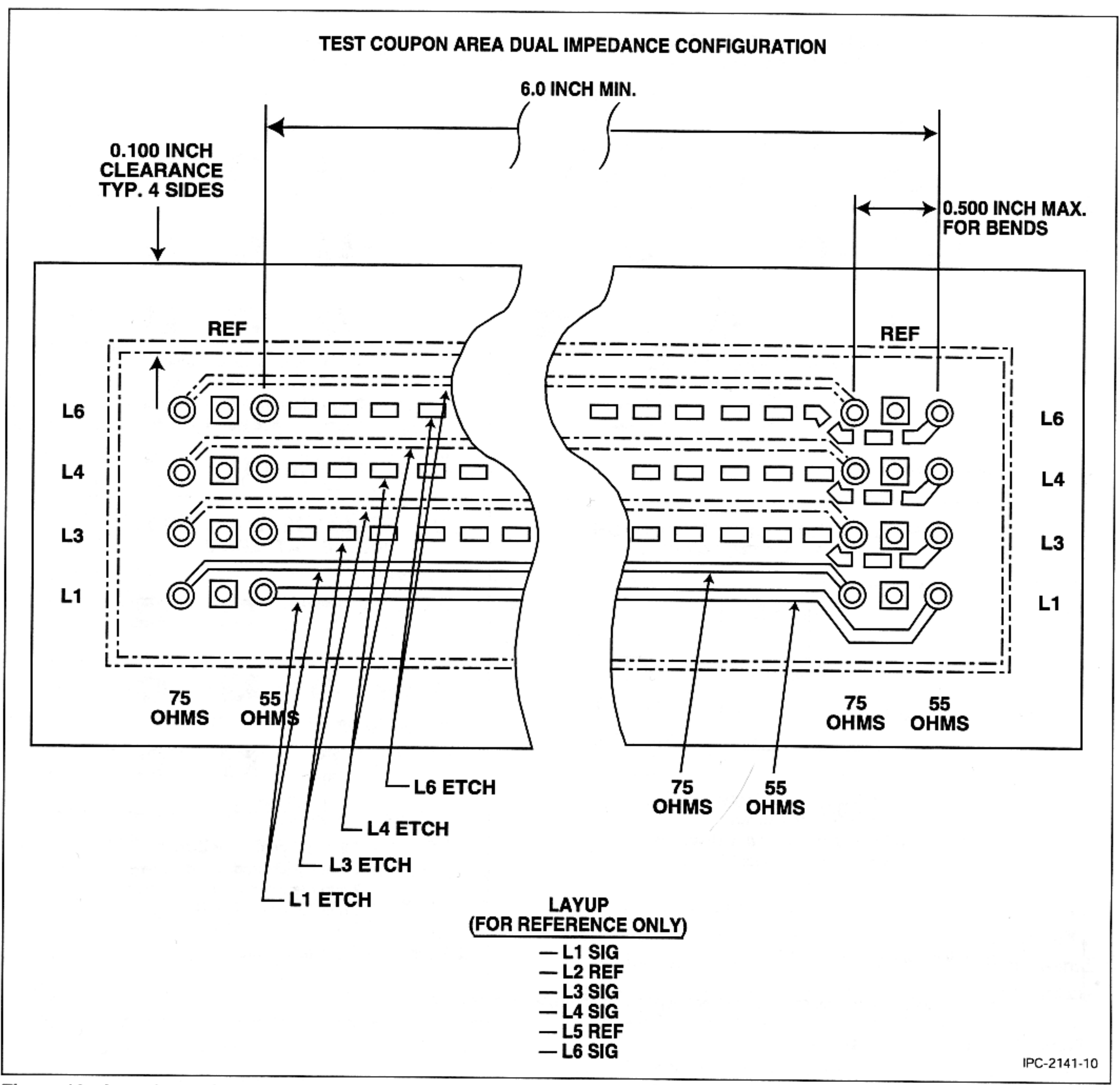


Figure 10 Impedance Control Test Coupon

which is composed of a broad spectrum of current frequencies, may require a combination of several low to high frequency capacitors. A single capacitor value or type typically cannot provide such a broad frequency.

4.8.2 Transient Capacitance Consideration

Switching transient capacitance provides very fast energy to charge the device during an output transition. This typically is the highest speed content of the wave form and requires the least energy. In very high-speed devices, the decoupling capacitance may be required to be built into the package to minimize the lead inductance between the capacitance and the device, or located nearby. If sufficient energy is not available, the signal transition time will degrade in the device.

4.8.3 Line Charging Capacitance

Line charging capacitance provides switching current to charge the signal conductor after the signal reaches it. The charge current is required until the conductor reaches its quiescent state. If insufficient capacitance/ current is provided the edge transition time will degrade.

Two types of line charging capacitance are required: one for capacitive lines and one for transmission lines. Capacitive line charging requires a relatively slower charging rate than a transmission line, but must provide more current. A

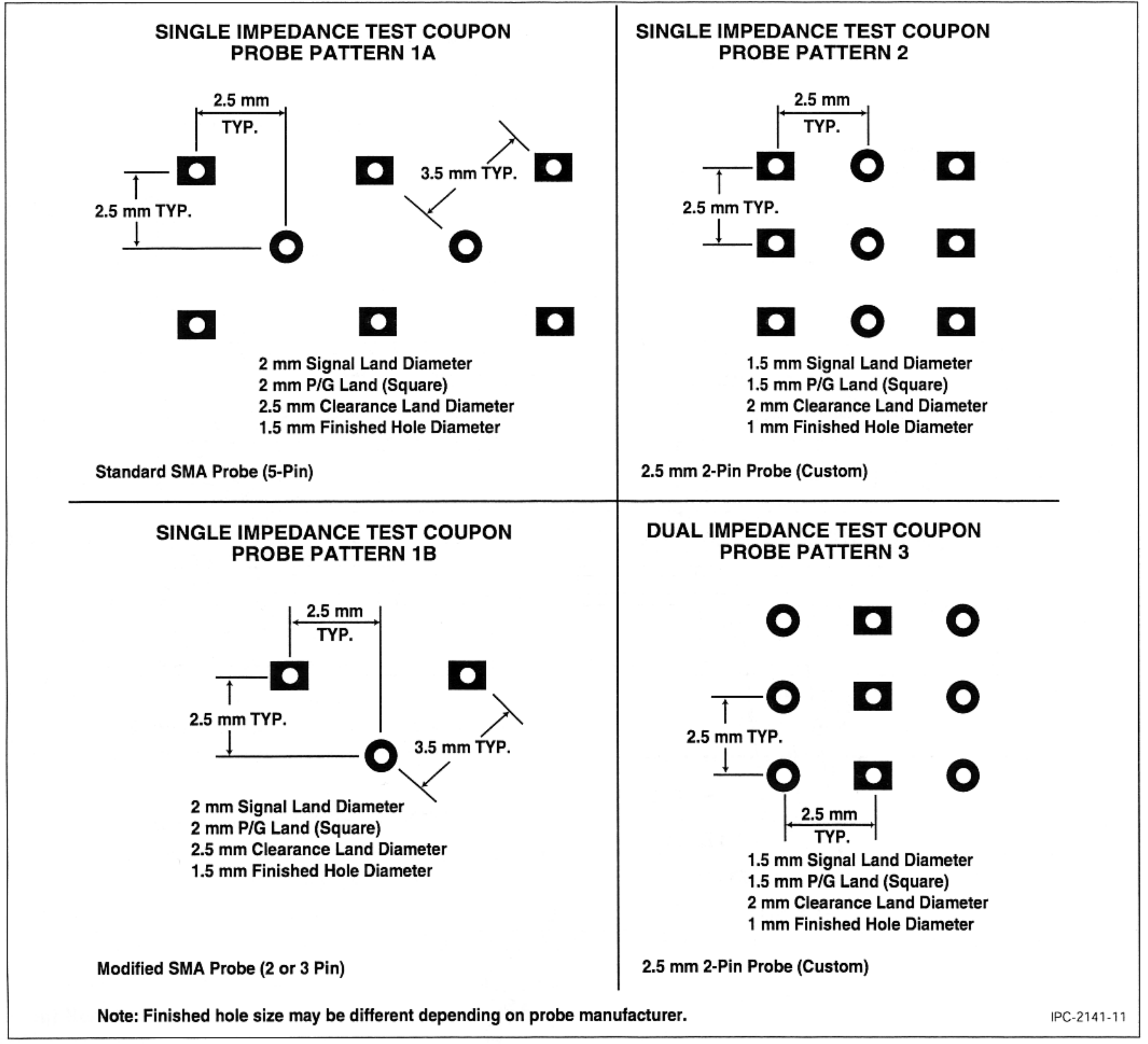


Figure 11 Test Probe Patterns

transmission line requires a slower, but typically longer, pulse to keep the line charged until all of the reflections subside.

4.8.4 Low Frequency (Bulk) Capacitance

Low frequency capacitance is often termed bulk capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors, and provide switching current to lower frequency requirements.

4.8.5 Capacitor Model

Capacitors with shorter leads provide current faster because the lead inductance is much lower. In high-speed designs changing the decoupling capacitors from leaded to leadless SMT capacitors can dramatically increase the circuit performance.

4.8.6 Decoupling/Capacitor Design Rules

a) Provide a high/low parallel capacitor network for the board, usually an electrolytic capacitor with high storage capacity and a ceramic capacitor for high frequency, located at the power input pins.

b) Provide local decoupling capacitors at each device. Larger devices with higher current demands may require more than one capacitor.

c) Use wider conductors for power and ground connections, reducing high frequency coupling. For SMT decoupling, connect the device to the capacitor with wide conductors.

d) Use short or wide connections to power and ground pins, reducing the inductive effects.

e) Use large area surface foil with multiple via connections to power and ground, reducing the inductive effects and providing a larger surface area than parallel via connections provide.

f) Divide use of decoupling proportionally to current supplied to the devices.

g) For optimum performance, connect capacitor terminals device leads directly to power planes; use 0.015″ vias and thermal reliefs with two connections to planes.

5.0 Design For Manufacturing

5.1 Process Rules in CAD

The design of high speed, high frequency circuits, using CAD systems does not vary significantly from conventional designs except that conductor width, conductor spacing, and plating thieves, may be added to the data base. Conductor widths are specified for certain nets to ensure that the nets have either the correct impedance or capacitance values.

Discrete wire CAD systems and routing software provide for wire conductor spacing, controlled wire lengths - both net nodes and entire net lengths - matched net lengths, minimum net lengths using concurrent orthogonal and diagonal routing, and other rules driven routing specifics.

Conductor separation in all axes is specified to ensure that nets have proper spacing relative to other nets for minimum noise/crosstalk.

5.2 Design Complexity and Correlation to Cost

Design complexity of high speed logic boards can be very simple as in microwave stripline or microstrip or they can be very complex as in a high performance, multilayer circuit board. Material selection may impact the cost.

The following are some of the cost drivers for controlled impedance/controlled capacitance boards:

1. Tighter impedance/capacitance tolerances than normal manufacturing processes will allow. The tolerance range is normally 10% to 15%.
2. Specifying parameters that cause suppliers to control both physical and electrical measurements. i.e., thickness of dielectric layers and impedance value for that layer.
3. Insisting on multiple impedance/capacitance values for the same layer. Increased scrap will result because another value may be acceptable while one value may be just out of range.
4. Not allowing the supplier to make adjustments that suit their processes, such as altering conductor width, dielectric thickness or laminate choice.

6.0 Data Description

Data should include the construction details on a layer by layer basis as well as the design data from the CAD system. Combined, the complete detail of the board fabrication should include the nominal values as well as the tolerances. Physical parameters as well as material properties should be included in the description.

6.1 Details of Construction

The following should be included in the data along with the tolerances for a complete description. Tolerances, either measured or as a reference should be specified:

a) Conductor width with its impedance value and/or capacitance value

b) Conductor thickness

c) Relative permittivity

d) Dielectric thickness

e) Soldermask type and thickness

f) Propagation delay

g) Layer diagram.

6.1.1 Controlled Construction

When physical parameters are specified, they control the build of the board. Values along with the tolerances should be:

a) Dielectric thickness by layer

b) Finished copper thickness by layer

c) Relative permittivity

d) Soldermask type and thickness

e) Conductor width and spacing

f) Layer diagram including overall thickness

By specifying these parameters, the board build and the performance is controlled by normal build parameters and their resultant tolerances. Conformance is verified by SPC/ inspection of the physical dimensions, not by measured electrical values. Controlled impedance values or capacitance values are not the criteria for acceptance.

6.1.2 Controlled Performance - Controlled Capacitance or Controlled Impedance

Controlled impedance/capacitance is the inverse of controlled construction, physical parameters are referenced (nominal) while performance values with their tolerance are measured:

a) Controlled impedance in ohms or controlled capacitance in pf

b) Propagation delay in picoseconds

c) Layer diagram including overall thickness

6.2 Isolation of Data by Net Class (Noise, Timing, Capacitance, and Impedance)

Identification of nets by class in either the net list or the CAD data base can allow specific conductors to be treated separately from the other conductors. As an example, two

conductors that are specified as a "noise susceptible" conductor and as a "noise generating" conductor, may have special physical spacing rules applied. Nets used for a particular class of logic, ECL as an example, could be isolated to a certain signal layer. Controlled impedance conductors should be assigned a unique conductor code (plotted width) so that they are treated separately from other conductors.

Different CAD systems and their routers should code or tag nets to accomplish routing and layer isolation strategies. By utilizing the features of the CAD system, high speed circuit design can be enhanced to meet design requirements.

6.3 Electrical Performance

In addition to meeting the predicted performance criteria, printed board designs must be manufacturable. Performance versus cost tradeoffs factor into the choice for optimum system design. Yields at manufacture are even greater contributors to cost than the obvious costs of raw materials and fabrication. For this reason, designers should be familiar with the materials available, their properties, capabilities, and tolerances and have a good understanding of process capabilities and tolerances that impact performance and manufacturing yield.

The development of a close working relationship with the engineering design group and board fabricator is of benefit to avoid prototype iterations which are costly and time consuming. Designing "based on previous experience" is certainly valid, but may be limited and not take full advantage of advances in both materials and fabrication. The development of a relationship with in-house materials and manufacturing groups or outside industry sources is advisable.

Electrical performance parameters should be established so that the measured acceptance values reflect desired performance. Since ε_r varies with frequency, measured values of ε_r should reflect the frequency of circuit or rise time of the devices. Critical clock line should have a length constraint consistent with skew requirements. Impedance values should reflect the characteristic impedance of the devices (chip set) and I/O lines should match the impedance of the connector/cable system. Noise levels should also be within the noise margin of the devices.

7.0 Material

7.1 Resin Systems

The resin systems used for circuit board laminates are classified into two basic categories: thermosetting and thermoplastic. Thermosetting resins are crosslinked matrices of smaller, polymeric units. The polar nature of materials generally contributes to higher relative permittivity, loss tangent (dissipation factor) and water absorption. The crosslinked structure of the thermosets generally provides better dimensional and thermal expansion characteristics. Water absorption becomes an issue because its relative permittivity is so high (approximately 75) compared to these resin systems. Relatively small changes in humidity in the environment may drastically impact performance (i.e., capacitance) and require strict environmental controls. Likewise, each resin system has a characteristic response of relative permittivity and loss tangent to temperature and operating frequency.

7.2 Reinforcements

Various reinforcements, supports, and/or fillers are incorporated with the various resin systems to enhance the physical or electrical properties of the composite laminate. A typical example is the incorporation of woven E-glass with a resin to enhance dimensional stability and reduce the X-Y coefficient of thermal expansion (CTE_{xy}) . Fillers may be added to modify the relative permittivity and/or to exclude resin and thereby reduce the overall CTE in X, Y, and Z dimensions.

7.3 Prepregs, Bonding Layers and Adhesives

Various thermosetting and thermoplastic materials are available for laminating a multilayer interconnect. Prepregs are woven glass supported resins in their B-stage, partially cured state. They are used to create the dielectric spacing between layers and are cured or crosslinked in the lamination process. This is the normal method of fabrication for multilayer boards. Other methods include thermoplastic bonding layers used for dielectric spacing that are fusion bonded during lamination by reflow at their melting point. Particularly in flexible board technology, thermoplastic bonding films and thermosetting adhesive films with thin unsupported materials are used where the dielectric is already provided by the base material.

7.4 Frequency Dependence

Figure 2 and section 3.4.3 define the material contribution through relative permittivity properties on impedance control. As concluded in that section, resin and the reinforcement used for laminate are key to the final relative permittivity properties of the material. Knowing the fabricator's materials and tolerances from the outset will go a long way toward predicting the probability that a given design will perform within the desired specifications.

8.0 Fabrication

A general understanding of the capabilities of board fabrication technologies and the realistic, achievable tolerances is critical to the successful implementation of designs. Areas of particular interest are the effect of processes and properties on manufacturing issues as they impact design considerations.

Knowing the fabrication techniques and tolerances from the outset will go a long way toward predicting the probability that a given design will perform within the desired specifications.

8.1 General

Generally, printed boards are custom components and cannot be treated in the same manner as normal "catalogue" components. Similarly, the printed board fabrication process is customized by each fabricator. Any comments or advice given in this document must therefore be modified to suit individual circumstances. The following are considerations to be taken into account:

a) Relative permittivity (ε_r)
The reinforced, supported, and filled materials are combinations of materials of different relative permitivities and will exhibit variations in this value unless the proportions of the combination are strictly controlled. The relative permittivity of the unreinforced materials should be invariant as these are generally uniform, isotropic materials.

b) Dielectric spacing (thickness)
Changes in the resin content will impact both thickness and relative permittivity. Thickness uniformity among materials will vary with the technology and the level of process control employed by the laminate manufacturer. It is impacted by choice of prepreg, bonding layers, film, and lamination conditions.

c) Prepreg
Prepreg thickness, and therefore relative permittivity, may vary with pressing conditions. For calculation purposes, the designer should consider the effective relative permittivity and thickness of a prepreg after the lamination cycle and account for any relative permittivity mismatches that may exist between the prepreg and other layers.

d) Conductor width and spacing
Conductor width and spacing will be impacted by artwork, imaging, copper foil thickness, etching and plating.

e) Conductor geometry
Conductor geometry may be influenced by imaging technique, cleaning, etching and plating, particularly on outer layers where undercut in thick foils with narrow lines will create trapezoidal shapes.

8.2 Preproduction Processes

The salient preproduction processes are shown in Figure 12.

8.2.1 Artwork Verification

The manufacturer may receive artwork in one or two forms:

a) Electronic data

b) Photo tools

8.2.1.1 Electronic Data

This is the preferred format; it can be input from a floppy disc or magnetic tape, or transmitted via modem. To enhance production the design rules employed during layout can be electronically compared to the relevant design rules in the host database library. Each layer will be identified by a unique file identity number. (See IPC-D-350 and IPC-D-356)

8.2.1.2 Phototools

Phototools are supplied as positives and/or negatives and are supported by relevant documentation i.e. drill tables and/or drill tapes, mechanical drawings. The material used is hydroscopic and must be stored correctly at a temperature of (23 ±2)°C and a humidity of (45 ±5)% RH.

8.2.2 Panelization

This is the stage where artworks are step and repeated and robber bars and test coupons, are added. Electronic data is manipulated for panelization and can be rotated and/or mirrored to assist current distribution and present edge connections, for subsequent gold plating, to the panel boundary.

8.2.3 Tooling

Tooling information is either derived from the electronic data files or may be supplied on magnetic tapes/disc. The tooling is specific to the fabricator. It may include pinning locations and coupons that are located outside the circuit area. The information can be transposed from the phototools via digitization and area measurement.

8.2.4 Plotting

The photographic film must be stabilized prior to use. The panelized electronic data is down loaded to a photo-plotter, where the light sensitive film is exposed. The exposed film is developed. These systems are usually automated by using a magazine/cartridge film feeder in the plotter which is then transferred to an auto feed developer. Plotting and developing are normally carried out in a controlled clean room environment.

8.2.5 Artwork Inspection

All artwork should be checked prior to use. It is the manufacturers responsibility to ensure that the production phototools are suitable to attain the end product. The following list identifies some of the criteria/parameters to be checked:

a) All layers present and correctly oriented

b) Each layer is uniquely identified

c) Contrast between clear and opaque areas

d) Registration/scale

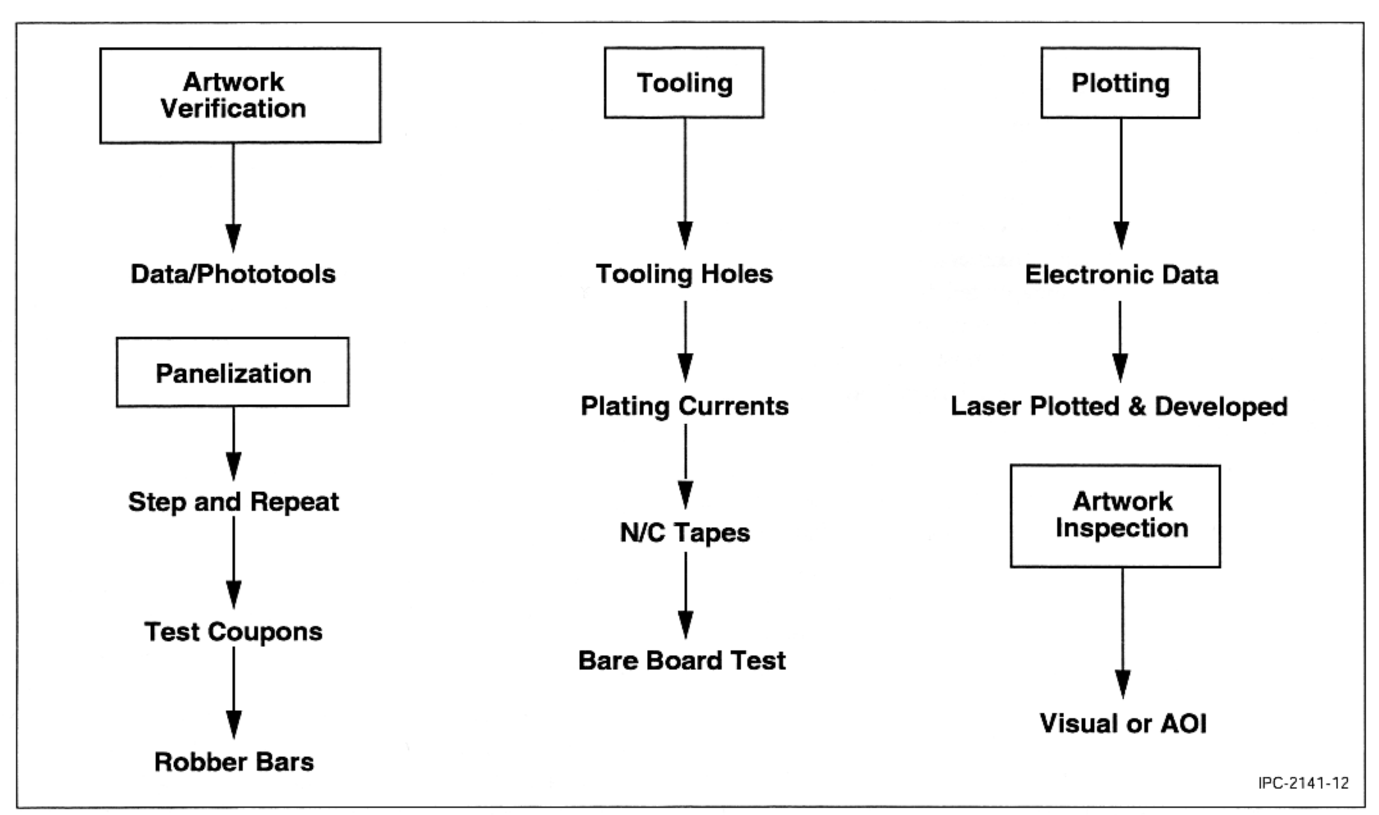


Figure 12 Flow Chart of Pre-production Processes

e) Geometry definition

f) Inclusions/pin holes

g) Land/hole ratio

h) Conductor/land clearances (gap width)

i) Annular clearances for ground and planes

The above list is not exhaustive but should be used in conjunction with the relevant customer detail specification.

8.3 Production Processes

A flowchart of the processes employed in the fabrication of a typical multilayer printed board is shown in Figure 13. Critical processes for controlled impedance are boxed.

8.3.1 Processing Considerations

The use of Statistical Process Control (SPC) is advantageous in the fabrication of printed boards. SPC becomes an absolute necessity for consistent impedance control. Process capability indices should be established for all critical processes.

8.3.2 Laminate, Expose & Develop Cores

Conductor edge profile is critical to impedance control. The presence of residual photoresist should be avoided.

8.3.3 Innerlayer Etching

The effects of over-etch or under-etch upon impedance can be demonstrated by substituting changes in conductor width into one of the many formulae for calculating characteristic impedance. The existence of etch factors must be accepted. Process capability must be known and etch factors established. The fabricator must define the limits of his capability and also the distribution of final conductor width for a range of nominal conductor widths and copper weights. These must be established for inner and outer layers. Etch factors are the responsibility of the printed board fabricator and should be considered in the design.

8.3.4 Scan (AOI)

Automated optical inspection will detect an imperfection in a conductor that may affect impedance performance. A 50 µm imperfection (nick) in a conductor, while acceptable when considering DC performance, may prove unacceptable in a circuit working at 2GHz.

8.3.5 Lamination

Final pressed thickness, retained resin content, and relative permittivity are influenced by a combination of pressing technique and choice of hardware. Hydraulic, vacuum assisted hydraulic and autoclave press capabilities must be established. The printed board fabricator must demonstrate that impedance calculations are valid for the chosen press. Mixing board designs in a single pressing batch is to be avoided.

8.3.6 Hole Formation

Drilled hole diameter and land hole ratio affect impedance. Where high speed signals are routed via two or more

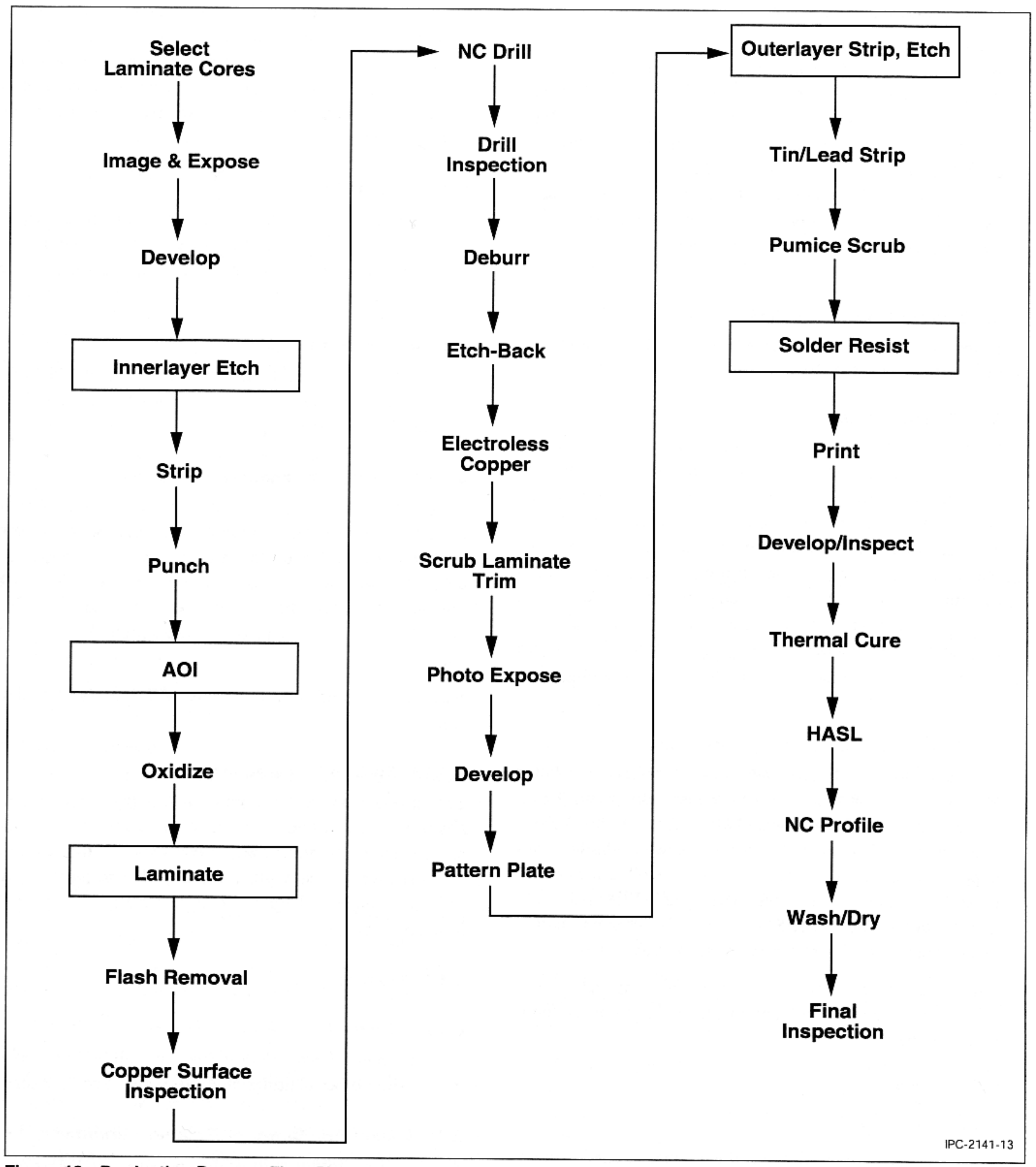


Figure 13 Production Process Flow Chart

impedance structures, the inherent capacitance of the via holes may affect the measured impedance although it is a second or third order effect. To minimize this effect, via holes should feature as small a drill / pad diameter as possible. Ground to via hole clearance lands should be as large as possible. Although these are mainly design considerations, the capability of the fabricator to routinely achieve the design should be established.

8.3.7 Photo Expose and Develop

Good photo exposure and development definition are an obvious necessity. The use of break away panels can be advantageous.

8.3.8 Electrolytic (Pattern) Plate

Good design practice should result in a balanced design with even pattern distribution across the circuit. When the design permits, the fabricator should be allowed to add plating thieves (robber bars) within the board area. Overplating, resulting in wider conductors is more detrimental than the actual increase in conductor thickness. This becomes a greater problem as conductor widths decrease. The use of panel plating or a combination of panel and pattern plating may prove a good compromise for some designs.

8.3.9 Outer Layer Strip, Etch

Stripping and etching processes are critical since any residue will destroy definition.

8.3.10 Solder Mask

Solder mask is only a consideration for surface microstrip impedance structures. The material may be considered to be a boundary layer. The printed board fabricator should determine in advance the individual derating factors for each solder mask type and thicknesses offered, and take these into consideration. The derating factors, commonly in the range of 1Ω to 3Ω, will depend upon the thickness and relative permittivity of the solder mask. Conformal coatings should be considered in the same manner. The degree of cure of surface coatings will also have a minimal effect on overall performance.

8.4 Impact of Defects at High Frequencies

It is common for limited numbers of defects in printed boards to be permitted where their distribution and prevalence is known. Examples include defects in conductors, whether printed or made from discrete wire, and spurious copper. Printed boards which feature controlled impedance must be virtually defect-free when judged against traditional criteria. The use of SPC is the only economic means of ensuring a consistently compliant product.

The influence of material properties upon impedance control should be understood, and the construction of the laminate specified.

8.4.1 Copper

8.4.1.1 General

The nature and condition of the copper (plated, rolled, annealed) will prejudice impedance. Given the "skin effect" at higher frequencies, conductivity is important. The relatively smooth surface of the die-drawn wire may provide better performance at higher frequencies.

8.4.1.2 Conductor Cross-Section

The surface of the copper conductor at the interface of the isolating substrate opposite the reference plane is a critical measurement. The cross-section profile (e.g.: trapezoidal for innerlayers, undercut for outer layers) of the conductor will influence the distribution of the electrical field around the conductor. Manufacturers attempt to provide as close to straight wall profiles as possible in order to control line width. The conductor shape by itself is a second or third order effect.

8.4.1.3 Pin-Holes

The traditional "neck down" or conductor nick permitted in conventional printed boards should not be allowed although conductor shape, in most circumstances, is a second or third order effect on controlled impedance values.

8.4.1.4 Spurious Copper

Spurious copper impacts distribution of the electrical field as the conductor configuration changes for the length that the additional copper is present.

8.4.1.5 Copper Thickness

Copper foils thicker than 17 μm are consistently supplied on the minus side of nominal. This assists the material supplier, but should be taken into account by the printed board designer who could be using erroneous figures for impedance control and current carrying capacity calculations. Foils at 17 μm and below are supplied at the nominal thickness.

Variation in conductor thickness will modify impedance slightly.

8.4.1.6 Surface Preparations

The smoother surface treatment of low profile copper foils has not been found necessary to achieve impedance requirements. A move away from existing foil treatment could reduce peel strengths, and any change must be carefully considered. There is no cost penalty if low profile foils are stipulated.

8.4.2 Substrate

8.4.2.1 General

The difference between localized and global defects and effects should be identified and corrective action taken.

8.4.2.2 Dielectric Constant (Relative Permittivity)

Relative permittivity is typically measured at 1MHz and is totally dependent upon the glass resin ratio for a particular resin formulation. Graphs are available which extrapolate relative permittivity versus frequency and temperature up to 1GHz.

It should be noted that the effect of relative permittivity upon characteristic impedance is often overestimated. The position of this parameter in the many mathematical formulae available limits its influence.

8.4.2.3 Loss Tangent

The dielectric loss of a substrate affects its use at high frequencies. Ceramic material has a high relative permittivity but its low loss properties make it suitable for some applications. For all logic families except GaAs, loss tangent is a third order effect and not of significant concern.

8.4.2.4 Laminate Consistency

Laminate suppliers will consistently press their products to the same standard. Any changes in glass styles or resin systems / styles MUST be discussed beforehand with the printed board fabricator.

Relative permittivity tolerance is usually in the region of ±0.15. Material thickness tolerance is generally ±10%, but the repeatability of an agreed build can be held to much tighter tolerances.

8.4.2.5 Prepreg

In order to control the Z-axis separation between conductors, thin laminate should be used in preference to prepreg. Where prepreg is used, it should be noted that the etched copper conductors will become impressed into the prepreg during relamination by the printed board fabricator. This reduction in pressed thickness must be considered when calculating the conductor separation, and will depend upon:

- — conductor width
- — copper thickness
- — resin content of prepregs
- — type of glass composition

8.4.2.6 Inclusions

Conductive inclusions in the laminate should be considered as spurious copper. Non-conductive inclusions will modify the relative permittivity of the substrate, and their effect will depend upon location, size and prevalence.

8.4.2.7 Voids

This type of defect, in common with delamination and crazing, will also affect relative permittivity to a degree determined by location, size and prevalence. In general, this type of defect will not be as serious as a copper defect.

8.4.2.8 Resin Flow and Content

The properties of the resin will have an effect upon the performance of the printed board. Once characterized, it is possible to allow for these properties. Suppliers of substrate materials experience little problem in producing single ply glass cores. Tighter thickness control (10%) can be achieved using single plies with less resin in the structure, without compromising product quality. Although no cost penalties are incurred, the higher glass resin ratio gives an undesirable higher relative permittivity.

8.5 Data Description

8.5.1 Type of CAD Data

All data for controlled impedance designs MUST be supplied in a digital format. A minimum of "Gerber" formatted files are required, but IPC-D-350 formatted files are preferred.

8.5.2 Customer Interface

Designers must meet with the printed board fabricator from the outset and a "design for manufacture" philosophy should be encouraged. Critical controlled impedance conductors must be identified. Agreements should be made defining parameters that can be varied, and to what degree.

9.0 Time Domain Reflectometry Testing

9.1 TDR Method of Choice

Time Domain Reflectometry (TDR) measurement is the recommended method of testing controlled impedance PWBs because it allows impedance variations along the length of the line under test to be measured. The fast rise-time output pulse simulates the operation of fast logic pulses in a functional test. Any reflected voltage indicates variation in impedance and can be used to calculate the lines characteristic impedance. See Test Method 2.5.5.7 of IPC-TM-650, Test Methods Manual.

Network analyzers which use frequency domain testing can also show variations of impedance against distance by utilizing digital signal processing techniques on the measured data (inverse Fourier transform). These instruments are an acceptable alternative to TDRs but they tend to be more expensive.

Other methods used such as micro-sectioning and capacitance testing of boards measure only some of the parameters influencing the characteristic impedance of a board. They also fail to show any variation in the lines characteristic impedance over its length.

9.1.1 Standard Test Coupon

It is recommended that a standard design for test coupons be adopted defining the overall dimensions, probe pattern per Figure 11, and fixturing holes. This will allow development of custom fixturing to maximize measurement repeatability and reproducibility.

Testing coupons in a custom fixture incorporating spring loaded coaxial probes is recommended to reduce errors in measurement. Temperature and humidity should be recorded with test results.

9.1.2 Types Of Test Specimen

A number of different controlled impedance structures may be used. These may be divided into microstrip and stripline configurations and also into single ended and differential signal paths.

If a suitable means of connection to signal and ground planes is available and the traces are suitable for testing then the actual controlled impedance tracks on the PWB

may be tested. Very short tracks or those with branches are examples of unsuitable test specimens.

Note: If it is not practical to test the actual conductors on the printed board then it may be possible to incorporate additional non functional conductors with suitable test points at each end. These should be on the same layers and be as representative as possible of the functional conductors and should be at least 125 mm in length.

Alternatively, additional conductors external to the PWB may be added in the form of test coupons. These should also comprise test conductors on each controlled impedance layer which are as representative as possible of the functional conductors. One advantage of external coupons is that they may be made to fit a standard test fixture.

Coupons may either be process related or design related. The former will consist of conductors of the appropriate impedance on each controlled impedance layer. Design related coupons may incorporate other circuit features such as 90 degree bends and via holes to assess the effect of these on the overall impedance.

9.2 Equipment

9.2.1 Time Domain Reflectometry Method

Factors affecting the consistency of TDR readings

The following factors have been found to adversely affect the quality of TDR measurements on controlled impedance PWBs:

a) Incorrect set-up and calibration of instrumentation
b) Different test methods and means of calculating impedance
c) Variation in manual positioning of cursors
d) Quality of impedance reference
e) Poor or intermittent probe connection during testing
f) Inadvertent reversal of signal and ground connections
g) Operators fingers on the coupon
h) External material in contact with the coupon
i) Inconsistent connection to stripline ground planes
j) Variation in manual probing technique
k) Ambient temperature and humidity

9.2.1.1 Method for Consistent TDR Testing

Use of software for automated instrument set-up and calibration is recommended. This can ensure that the test system is correctly and consistently configured to perform testing. In addition it can calibrate the system on every test minimizing the effects of instrument drift.

A standard test procedure and method for calculating impedance from the TDR voltage/time trace should be agreed upon. This equation may then be incorporated into the system software.

The region over which the printed board conductor is to be tested should be defined in the system set-up. This should be chosen so as not to include the impedance variations normally seen at the probe to test conductor interface and the open circuit termination. Typical from 20% to 85% of test coupon distance.

Pass/fail testing may be achieved by checking that the impedance is within a given tolerance of its nominal value over the length of this interval. Mean and standard deviation of measured impedance along the tested region should be recorded.

A precision airline reference impedance may be used to improve system accuracy. This is connected in series with the printed board under test and used for system calibration. A reference impedance close to the nominal impedance under test gives the best results.

Probes, cables and connectors should be of high quality and suitable for high frequency signal transmission. A standard footprint for probe connection should be adapted to reduce the current requirement for multiple probe types. The commonly used SMA connector (one ground pin only)is suggested. RF work may be better done with four (4) gold ground pins.

Another problem is that for consistent and accurate measurements a high degree of manual dexterity is required.

Fixturing has been developed for test coupons to ensure consistent probing action and minimize operator induced errors in measured impedance. The fixture also allows faster testing of coupons with multiple tracks. A hand held assembly using the same probe technology could also be developed for testing controlled impedance conductors within the printed board.

9.2.1.2 Test Equipment Specification

Time Domain Reflectometry uses a fast step output pulse generator combined with a high bandwidth sampling oscilloscope. The step pulse is applied to the printed board conductor and the reflected voltage is monitored by the sampling oscilloscope. Any changes in characteristic impedance cause reflections in voltage which can be used to calculate the impedance of the transmission medium at a given distance from the TDR.

9.2.1.3 Rise Time & Bandwidth Requirement

A step output time domain reflectometer (TDR) is required with a system bandwidth and rise time sufficient to measure the length of the conductors to be inspected. A shorter rise time and higher bandwidth is required to measure the impedance of shorter conductors. System rise time (t_r) in picoseconds and bandwidth (BW) in gigahertz are related by the equation:

$$BW = 0.35/t_r$$

A fast rise time indicates the presence of high frequency harmonic content. The step effectively tests the printed board over a range of frequencies from around 500 MHz to the bandwidth of the instrument.

These parameters reflect the overall system performance resulting from the combination of the TDR's sampling oscilloscope bandwidth and the pulser output rise time. Reflected rise time is the time taken for a 10% to 90% transition resulting from a reference termination at the instrument's front panel connector.

For example a 200ps reflected rise time TDR has a system bandwidth of 1.75 GHz and is capable of measuring conductors of 3 inches and longer. The rise time of the waveform will obscure approximately one inch at the beginning of the TDR signature.

A 35ps reflected rise time TDR has a system bandwidth of 10GHz and is theoretically capable of measuring PWB conductors of quarter of an inch in length. In practice however one meter of typical flexible coaxial cable will slow the observed rise time considerably and aberrations at the probe to line interface will prevent accurate measurements on the first inch of the coupon.

9.2.1.4 Step Flatness

In addition to fast rise time the system must have a well defined pulse output in terms of deviation from a perfect step. Practical TDR systems will exhibit some aberrations from the ideal waveform just prior to and after the step. These aberrations will also be seen in the reflections caused by any changes in impedance such as the step from a 50 Ohm probe into a 75 Ohm coupon. Since the impedance is calculated from the amplitude of the reflected voltage these aberrations must be small over the tested region of the conductor for accurate impedance measurement.

Typical TDR specifications give maximum aberrations of ±3% of step amplitude in the critical area of around 1ns or approximately 100 µm past the step. These are significant when there is a large reflection coefficient at the probe to printed board interface. This could theoretically cause an error of just under ±1 ohm when measuring a 75 ohm conductor with 50 ohm reference.

Fortunately, typical aberrations are usually much better than the specification, some of the high frequency aberrations are filtered out by the cabling and averaging the impedance measurement over some distance will cancel out some of the errors.

9.2.1.5 Other Parameters

a) Minimum pulse amplitude of 200mV

b) Vertical resolution of at least 0.1% of pulse amplitude

c) Vertical accuracy is not critical as the impedance is calculated from a ratio of voltages

d) The vertical linearity of the measurement system is important but will not normally be specified

e) A vertical accuracy of 2% of pulse amplitude (maximum) should be sufficient

f) Offset drift and gain variation of the displayed step should be less than 0.25% of step over one calibration period

g) Horizontal time base resolution of at least 25ps (equivalent to 0.1″ at Vp = 0.66 * c)

h) Horizontal accuracy is not critical for impedance measurements but may be of interest if propagation delay measurements are to be made with the equipment

i) Horizontal drift should be no more than 100ps for consistent measurements

9.2.1.6 Protection

Since the TDR instrumentation is very sensitive to static damage it is recommended that some form of protection is used. Some TDR systems have internal protection diodes to prevent static damage but higher performance systems usually require an external static isolation unit.

9.2.1.7 Test Procedure

Impedance is normally calculated by comparing the voltage reflected from a known impedance reference and the line under test. The reference impedance can be internal to the instrument or external as shown in Figure 14.

$$Z_{line} = Z_{ref}[V_{line}/(2V_{ref}-V_{line})]$$

A plot of impedance against distance over the length of the coupon may be generated by applying this formula to the voltage time waveform acquired from the TDR. A typical plot is shown in Figure 15.

In order to achieve accurate measurements the impedance of cabling and connectors up to the probe and reference should be 50 ohms. Thus the reflection from the reference to the coupon is the first major impedance discontinuity.

Calibration to the internal impedance of the TDR instrument is attractive in that it does not require the operator to have the correct cabling and impedance reference connected to ensure good calibration. Calibrating to a reference impedance close in value and proximity to the printed board offers improved accuracy.

9.2.1.8 Differential Test

Differential impedance structures and measurements are currently much less common than single ended ones. With ever increasing requirements for high frequency performance it is likely that the improved signal to noise ratio of differential signal paths will make these structures more common.

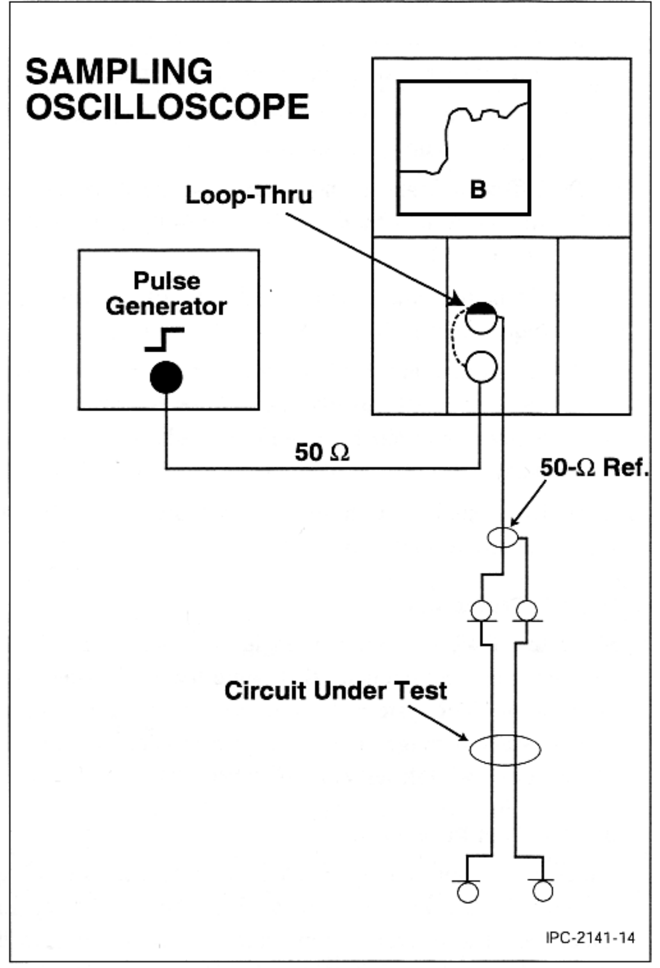


Figure 14 Typical TDR Test Set Up, Unbalanced Line

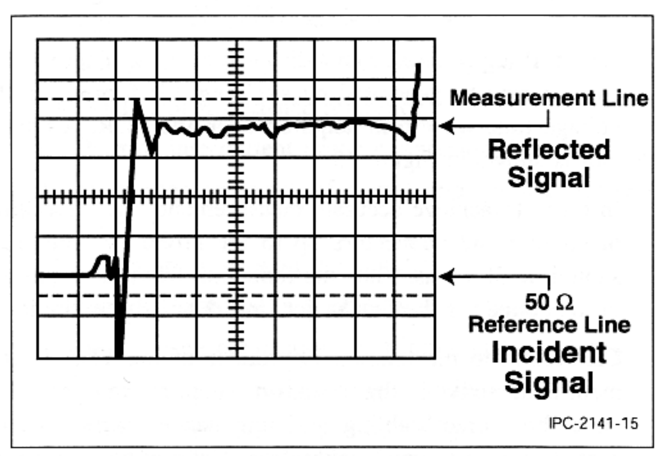


Figure 15 TDR Waveform

The main difference between this and single ended TDR is that differential structures require pulsing and sampling on two lines instead of one. Much of the above work on factors affecting the consistency of TDR readings will still apply but more advanced instrumentation, different impedance calculations and different probes and test fixturing are required.

Three methods exist for testing differential impedance. In true differential TDR, two very closely matched pulses of opposite polarity are simultaneously transmitted down balanced conductors and applied to the test coupon. The reflections are monitored on a sampler on each conductor. Valid differential measurements can also be achieved using one pulse generator with two samplers and alternatively, one pulse generator with one sampler. These two methods make individual measurements on each conductor and then mathematically combine the results to calculate the resulting differential impedance. Simultaneous connections are made to both conductors in these two methods despite there only being one stimulus (illustrated in Figure 16).

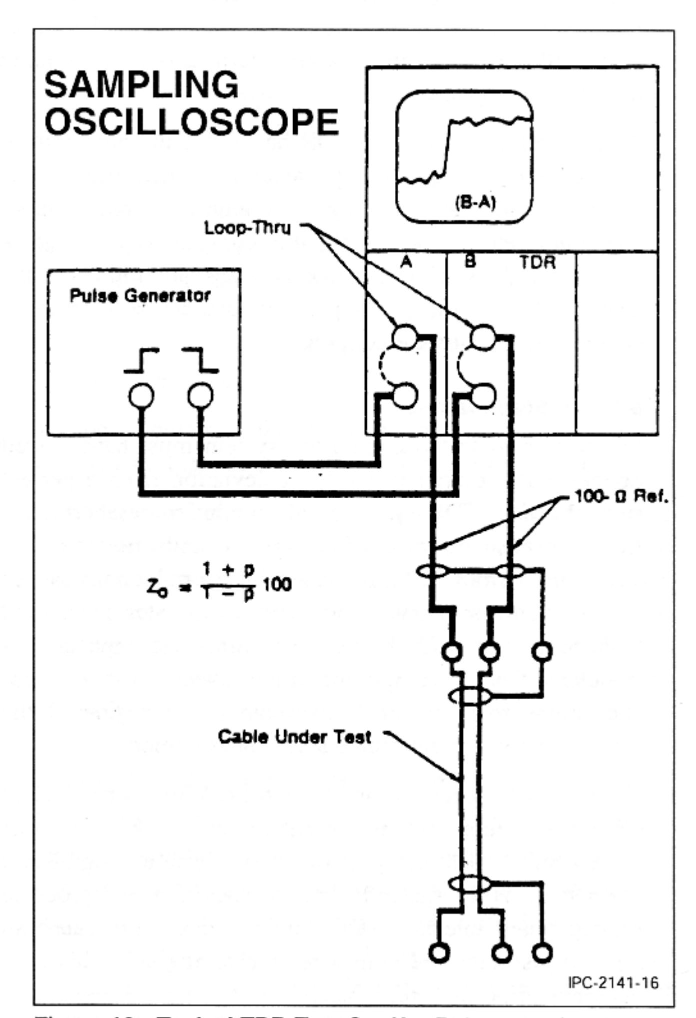


Figure 16 Typical TDR Test Set Up, Balanced Line

Figures 17, 18 and 19 show an alternate test setup based on a MS-DOS based PC Controller/display. Figure 17 shows the setup for a single, unbalanced test while Figure 18 shows a dual conductor balanced test. Figure 19 shows the unbalanced line display presentation.

It is anticipated that further work on differential impedance testing will be required in the future.

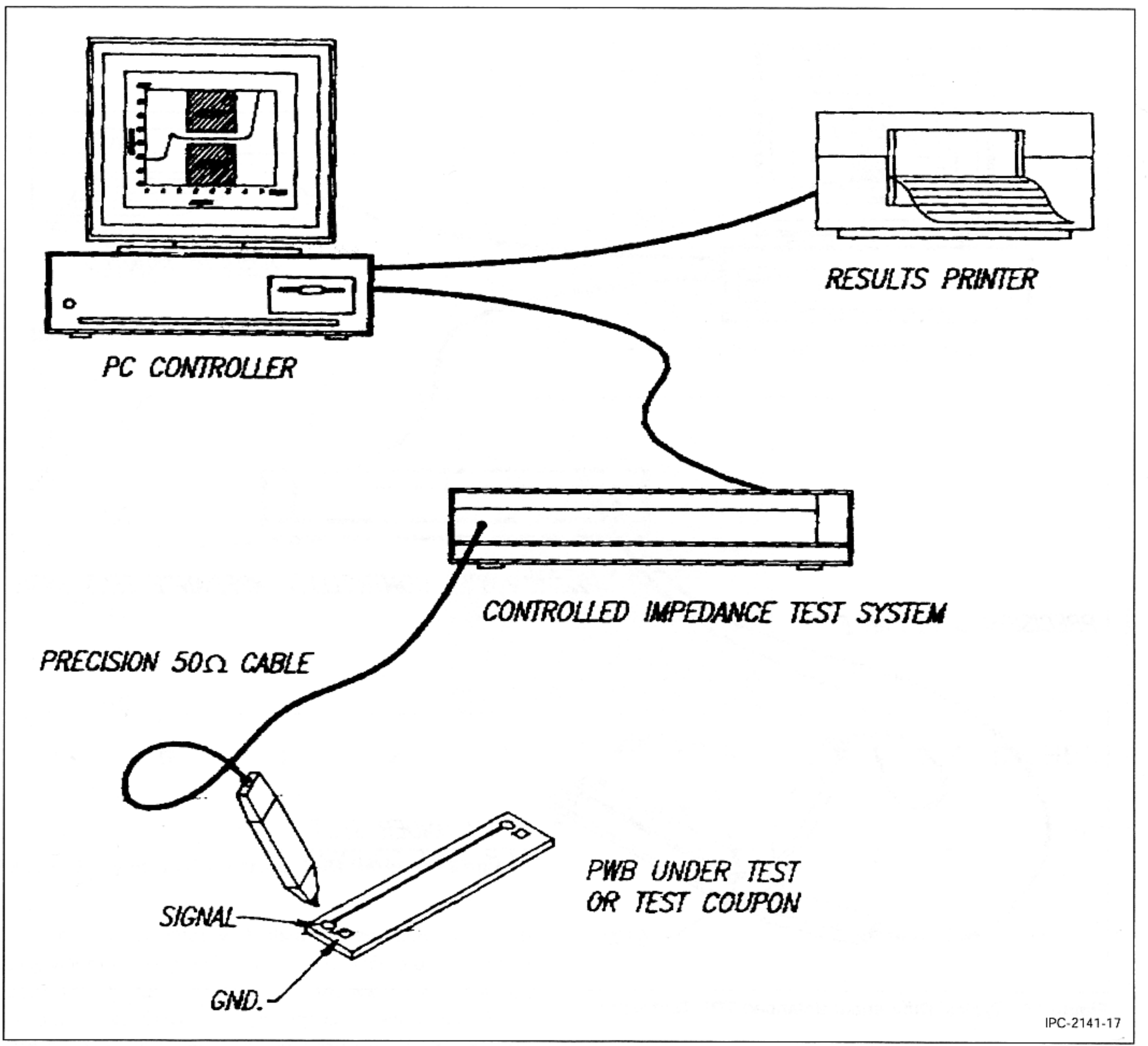


Figure 17 Typical Single Ended Unbalanced TDR Test Setup

9.2.2 Calibration Techniques

9.2.2.1 Cables

High quality 50 ohm coaxial cables should be used to minimize the attenuation of the high frequency components in the fast rise time pulse. Cable lengths should be kept as short as practically possible for the same reason.

9.2.2.2 Reference Impedance

High quality coaxial air lines provide the best impedance references. These should be checked periodically to national standards. The test instrumentation should also be calibrated regularly. A 'gold' coupon with a number of conductors of known impedance may also be useful for comparison of different test systems and as a test for correct instrument operation.

9.2.3 Standard Test Probe and Fixture

9.2.3.1 Connectors

High frequency 50 ohm connectors should be used to minimize impedance discontinuities between the TDR system and the printed board under test. SMA and GR connectors are suitable HF connectors.

9.2.3.2 Probes

SMA connectors are a commonly used form of probe. These may be used as supplied with four ground connections and a central conductor all on a 0.1" (2.54mm) grid. Alternatively three of the ground pins may be removed to make a two prong probe. For a more consistent probing action in a test fixture a spring loaded coaxial probe may

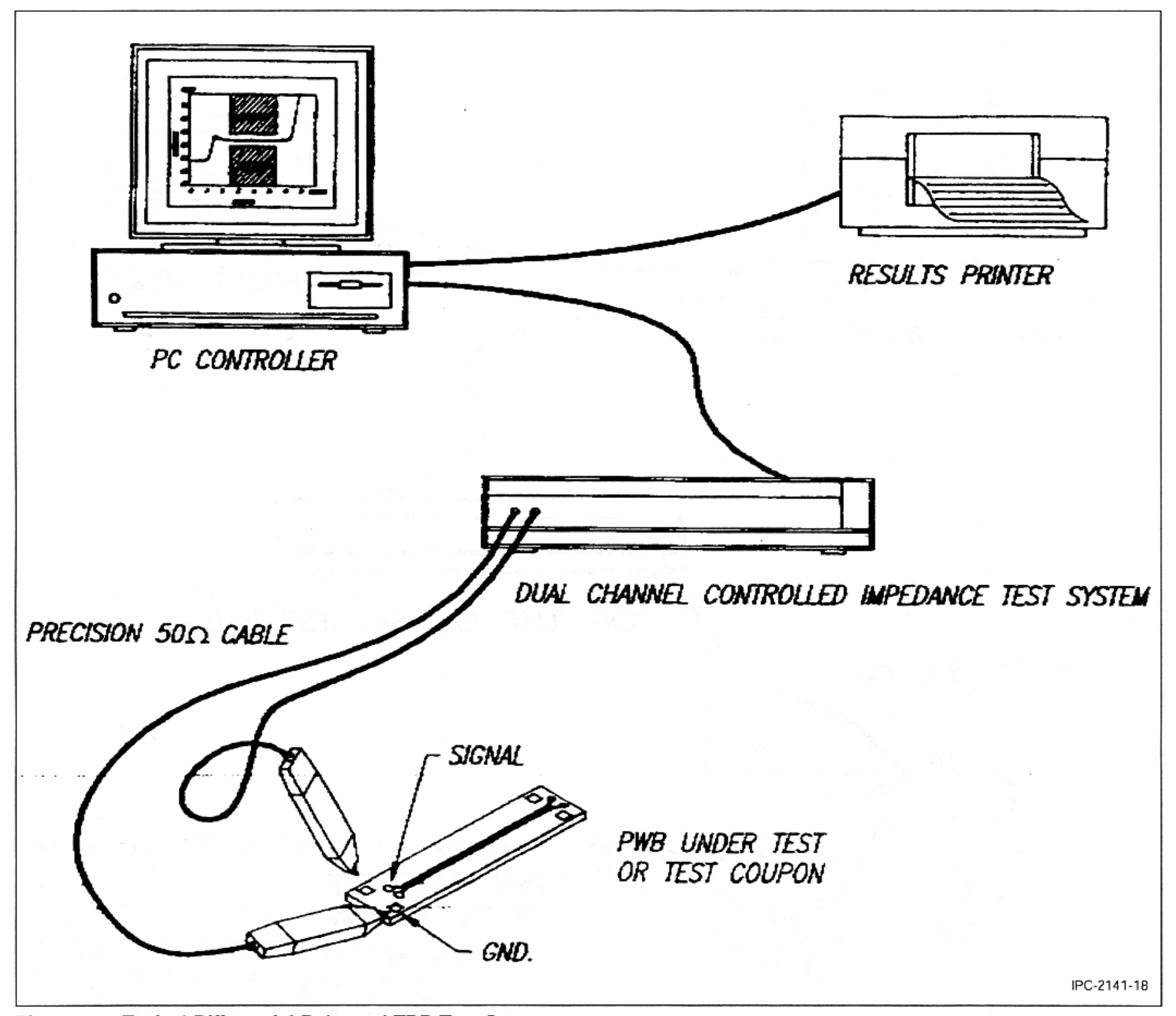


Figure 18 Typical Differential Balanced TDR Test Setup

be used. This type of probe can be adapted to match the same SMA type land pattern.

9.2.3.3 Fixturing

In order to reduce operator induced variations in the testing of coupons a prototype test fixture has been developed incorporating a spring loaded coaxial probe on a sliding carriage. A standard test coupon may be placed in the fixture for testing. Tooling holes ensure that the coupon is correctly oriented and the board is supported at each end leaving the active portion in free space. The probe carriage is manually located at indexed positions which match the coupon land pattern.

9.2.4 Correlation of Equipment Types and Laboratories

9.2.4.1 Correlation Of Different Equipment Types

Extensive correlation of various TDR and Network Analyzer test equipment has been carried out as well as repeatability and reproducibility studies on individual instruments. Variations between systems are typically of the order of 0.5 ohms for impedances of 50 ohm lines and 1 ohm for 75 ohm lines. A significant portion of this is thought to be due to the different means of setting up calibrating and performing measurements on different types of equipment. Use of common software to control the various instruments could improve these figures by ensuring standard set up, calibration and measurement technique.

9.3 Training

9.3.1 Operator Skill Level

Many existing TDR systems are highly complicated and require highly skilled staff to correctly set up, calibrate and

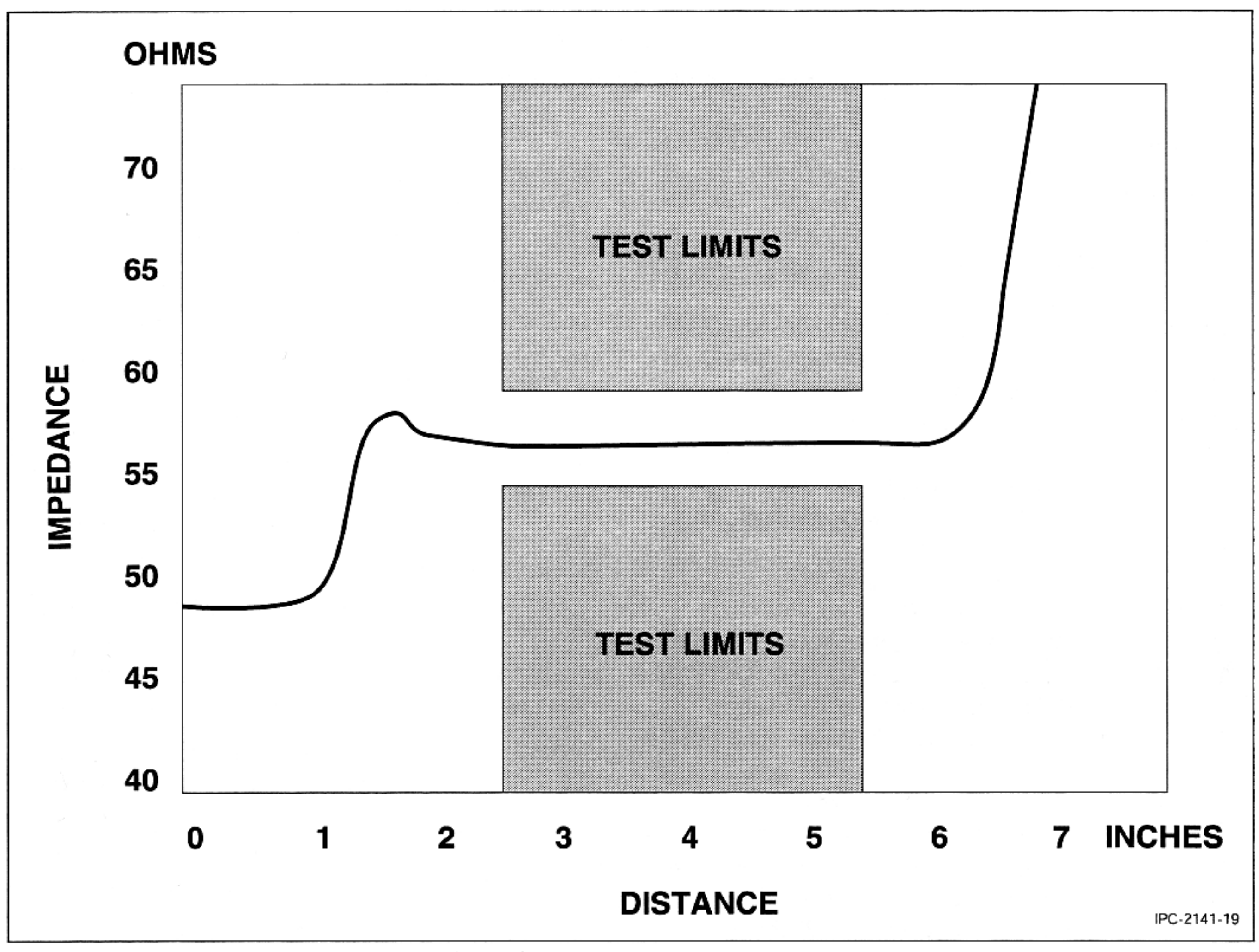


Figure 19 Typical PC Controller TDR Waveform Display

perform measurements with them. In addition test procedures are often long and complicated. This problem can be addressed by using specialized software for automatic instrument set. Once a test set-up has been stored all the operator need do is select that test and execute it. The software sets up the instrument, calibrates it, performs the test and displays the result. A direct plot of impedance against distance can be displayed plus mean standard deviation, minimum and maximum impedance. The PWB can be passed or failed according to whether its impedance is within tolerance over the tested interval. This approach requires minimal operator skill once the software is correctly installed.

9.3.2 Operator Knowledge

The operator must understand the test equipment being used for the test as well as its calibration procedure. In the case of programmable test equipment, an understanding of the program used for measurement is desirable. Board construction and its relationship controlled impedance is also desirable.

Appendix A
Units, Symbols, and Terminology

1 Symbols

Symbol	Description
AC	Alternating Current
Circuit Board	Includes Printed Boards and Discrete Wire Boards
CMOS	Complimentary Metal Oxide Semiconductor
DC	Direct Current
DIP	Dual In-line Package
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
FR-4	Epoxy Glass Dielectric Material
IC	Integrated Circuit
SMT	Surface Mount Technology
Tan(~)	Dissipation Factor (Loss Tangent)
TDR	Time Domain Reflectometry
T_p	Total Signal Line Propagation Delay Time
T_{pd}	Propagation Delay Per Unit Length
T_r	10%-90% Edge Transition Time (Rise or Fall)
TTL	Transistor-Transistor Logic
Z_o	Characteristic Line Impedance (Unloaded)
Z_o'	Characteristic Line Impedance (Loaded)
ε_r	Relative Permittivity
ε_r'	Effective Relative Permittivity

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